Avalanche and Short-Circuit Robustness of High Voltage SiC DMOSFETs

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SiC MOSFET Design Considerations

- Low Drain-Source Resistance, RDS,on
- Low Gate Charge, Input and Output Capacitances
- Robust Design for High Avalanche Ruggedness
- Low conduction loss at high temperatures
- Intrinsic diode with low reverse recovery charge
- Low Costs at high temperatures

Standard DMOSFETs for highly uniform production and robust and reliable performance
Due to low channel mobility, MOSFET design points are constrained

- **Small Channel Length** => Needs low Electric Field at Oxide => Smaller JFET Length => High Rdson
- **Under Short Circuit conditions**, High Electric Field at Oxides Observed
- **Different Layout schemes** can be employed to trade-off Rdson/Short Circuit/Avalanche parameters
Leading 4000 V/40 mΩ MOSFETs produced

- 4000 V/40 mΩ MOSFETs fabricated on 150 mm wafers
- Chip Size = 8.9 mm x 4.82 mm
$R_{DS,ON}$ for various designs

- $R_{DS,ON}$ reduces with increasing JFET spacing
- Higher JFET doping has clear impact in reducing $R_{DS,ON}$

- $R_{DS,ON}$ increases with increasing $L_{ch}$
- Higher variation in $R_{DS,ON}$ observed in devices with low JFET doping
Leakage current ($I_{DSS}$) for various device designs

- No significant impact of JFET Doping on $I_{DSS}$
- Median $I_{DSS}$ is higher for wider JFET spacing, for devices with higher JFET doping

- Median $I_{DSS}$ values are $< 30$ nA at $V_{DS} = 2400$ V
- No significant impact of $L_{CH}$ on $I_{DSS}$
Gate leakage current \( (I_{GSS}) \) for various device designs

- **Median \( I_{GSS} \) values < 1 nA for all designs**
- **No impact of JFET doping on gate leakage current**
- **Very slight statistical decrease of \( I_{GSS} \) observed for longer channel DMOSFETs**
Threshold Voltage ($V_{TH}$) for different device designs

- **No impact of JFET Doping on $V_{th}$**
- **$V_{th}$ is only weakly dependent on the JFET Spacing**

- **Clear dependence of $V_{th}$ on MOS channel length is observed**
- **$V_{th}$ reduction at lower channel lengths is due to the DIBL effect**
Double Pulse switching characterization

- VDS fall time = 30 ns achieved for switching at 1800 V and 6 A, with +20 V drive voltage and \( R_{\text{G,ext}} = 10 \ \Omega \)
Double Pulse switching characterization

- VDS rise time = 30 ns achieved for switching at 1800 V and 6 A, with -3.3 V Gate Drive Voltage
Negative Drain bias characteristics

- The negative drain bias (synchronous rectifier mode) performance of the DMOSFET at 25°C and 150°C is shown.
- Depending on the magnitude of the gate bias and the junction temperature, the device operates in either purely bipolar mode, purely unipolar mode, or in a mixed-mode.
Avalanche robustness of 4600 V DMOSFETs

- Short-Circuit and Unclamped Inductive Switching (UIS) tests are widely used to define the SOA limits of power devices.
- Avalanche ruggedness of a power device is determined by its ability to dissipate avalanche energy (EAV) without catastrophic device failure.
  - Both single-pulse and repetitive avalanche ratings are important for ultra-fast SiC power MOSFETs, since high voltage overshoots can be generated due to high dI/dt during device turn-off.
- An avalanche rugged device enables snubber-less converter design, leading to drastic reduction in cost, # of components and converter size.
- Automotive applications such as anti-lock braking systems and engine control units require power devices to dissipate more energy.
Single pulse avalanche energy

- SiC MOSFET successfully conducts a single-pulse avalanche energy (EAS) of 1.07 J (14.1 J/cm² normalized to the total chip size), at a peak drain current of 5.5 A, and drain voltage of 5100 V.
- An EAS of 14.1 J/cm² is among the highest ever recorded for a SiC MOSFET.
Stability of electrical characteristics after repetitive avalanche stress

- 200 mJ, 1000 cycle repetitive Avalanche Tests
- Minor degradation of Drain Leakage current
- No degradation (not shown) of output, transfer and body diode characteristics as well
Many Applications demand Short circuit capability - for certain period of time (5-10 $\mu$sec), the MOSFET should survive application of BUS voltage at near-full current.

Particularly challenging for SiC MOSFETs because short-channel makes output conductance poor (Saturation current increases with Drain Bias).

Sophisticated behavioral models developed by GeneSiC to estimate energy deposited into the device for various short circuit times.
Impact of channel length and JFET parameters on short circuit times

- Increasing Channel length, and other parameters improves Saturation characteristics of MOSFET, which limits Drain Current and hence longer Tsc
- However, RDS penalty ensues
Impact of gate bias on short circuit failure

- A good solution is limiting the Gate Drive Voltage to 15 or 16V instead of 20V
- Short Circuit Times can be enhanced by reduced Gate Biases
Impact of short circuit on device characteristics

- Not much degradation of MOSFETs after short circuit pulses applied
- 1000 cycle tests of 6usec pulses show no significant degradation of MOSFET characteristics (not shown)
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<tr>
<th>Rated Blocking Voltage (V)</th>
<th>R&lt;sub&gt;DS(ON)&lt;/sub&gt; (mΩ)</th>
<th>Maximum Continuous Current Rating</th>
<th>TO247-3L</th>
<th>TO247-4L</th>
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Conclusions

• Well-rounded SiC MOSFET design that optimizes performance, robustness and reliability produced

• Design Parameters correlated with on-resistance, short circuit and avalanche characteristics

• GeneSiC ready to sample 3300 V/40 mOhm SiC MOSFETs to select US-based partners

• AEC-Q101 qualified parts available through Industry’s leading distributors for Automotive, Industrial and Light Industrial
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