Overview of

PSMA TECHNOLOGY REPORT

3D Power Packaging
With Focus on Embedded Passive Component and Substrate Technologies

February 2018

PSMA 3D Power Packaging Phase III
A Special Project of the
PSMA Packaging Committee

Introduction

In 2013 the Power Sources Manufacturing Association (PSMA) Packaging Committee began what turned into a 5-year study of the feasibility of using 3D packaging to decrease the size and cost while increasing the performance of power sources. In 2014 the first Technology Report entitled "3D Power Packaging" was published. It surveys all know technologies at that time that appeared feasible for 3D Power Packaging. The conclusion of that report was that embedding components (active and passive) with in the substrate was the most viable technology for meeting the design goals for 3D power packaging. A Phase 2 report entitled "Current Developments in 3D Packaging with Focus on Embedded Substrate Technology" was published in March 2015. The report covered known substrate and component (active and passive) technologies that are available and roadmap technologies that should be watched. The phase 2 report concluded the largest gap for full implementation of embedded technology for power sources was the availability of passive components. As a result, the PSMA packaging committee commissioned a Phase 3 report to be written and research by Georgia Tech Packaging Research Center (GT-PRC) in June 2017. The Phase 3 Technology Report entitled "3D Power Packaging with Focus on Embedded Passive Component and Substrate Technologies" was published in March 2018. This report covers in detail passive component (capacitors, inductors, resistors) available for embedding and 3D Packaging looking at power levels up to 100 kW. It also provides an update to 3D packaging technologies in production at the time of the report and future trends for both the components and manufacturing technologies. All of the above-mentioned Technology Reports are available from PSMA on their website www.psma.com . This article will provide a short summary of the Phase 3 report, a view of the table of contents and excerpts from each chapter to give the reader a glimpse of the report contents.

Phase 3 Report Summary

The Phase 3 report is the third in a series of reports focusing on using 3D packaging to reduce the size and improve the performance of Power Sources. The focus of this report in on passive and substrate technologies. Miniaturization of passive components without compromising their power handling and efficiency, and their integration with actives has always been a key focus for power packaging. There is also an increasing trend to vertical or 3D package integration to address the performance issues by eliminating parasitics from large leads. Wide bandgap (WBG) devices, on the other hand, have become a key enabler to achieve high power densities and efficiency, owing to their many advantages over silicon. In particular, they enable operation at higher switching frequencies and temperatures with subsequent improvements in power density and efficiency. While SiC is presently the most mature WBG technology, production-ready for power train applications, GaN devices have recently gained importance with the GaN-on-Si technology, to reduce the cost. Embedding of WBG actives and passives, therefore, has become a very important technology in power applications to increase power density and efficiency along with miniaturization of power modules. Embedding gives lowest

package inductance and enables co-integration of power systems and drivers in a single package with direct interconnection between gate driver circuits and switches with shortest interconnection length. This, however, leads to several process integration and reliability challenges that need to be systematically addressed. The challenges vary depend on the power of the system, power density, operation temperature and other criteria. The power electronics industry is actively pursuing solutions to address these challenges.

GT-PRC and PSMA have systematically surveyed the recent advances in passives, active embedding and 3D passive-active integration to generate this report, with emphasis on 3D power packaging enabled by advances in passive components and embedding of actives in power packages. A detailed literature study was conducted on key advances in embedded passive technologies and related topics. Emerging nanomaterials and processes are described for inductors, capacitors and resistors. Nanostructured materials provide additional degrees of freedoms in enhancing the properties to improve the performance metrics such as volumetric density and efficiency of the components. Key enabling building-blocks are described for each technology. The manufacturing challenges are also highlighted in advancing the components to improve performance. Industry leaders were surveyed to get the recent technology advances in each category. Roadmaps are projected for passive component advances and active embedding technologies.

Passive components, substrates and packaging technologies are categorized as follows. Magnetic materials are classified into three categories: a) low-frequency, high-power magnetics such as those used in isolated DC-DC converters, b) medium-frequency, medium-power inductors used in ultra-thin or embedded inductors, c) high-frequency magnetics used in integrated power module applications. Similarly, capacitors are classified into: a) formed thin-film capacitors for high-frequency decoupling, b) high-surface area silicon trench, sintered porous tantalum capacitors or etched Al foil capacitors, c) inserted ultra-thin MLCCs, and d) high-voltage, high-temperature capacitors. Resistors are classified into thickfilm and thinfilm resistors and the key materials and process advances in each class are highlighted.
The trends in 3D power packaging are also described in three categories: low power (1-100 W), medium power (100-1000 W) and high power (10-100 kW). Integration in each category is classified into lead-frame-based, substrate-embedding based, and traditional ceramic substrates. Active embedding with panel- scale substrate manufacturing is also reviewed in detail. Recent innovations in substrate materials and associated reliability challenges such as via cracking, dielectric cracking or electric breakdown are highlighted. Advances in die-attach solutions with sintered nanocopper are reviewed, highlighting the evolution of low-stress sintered copper-based die-attach solutions.

In summary, a comprehensive industry report on recent advances in 3D power packaging, enabled by advances in passives and active embedding is generated for PSMA.

Table of Contents from Phase 3 Report

Excerpts from CAPACITORS Chapter

Excerpt from Introduction

Capacitors are critical components in any electronic system. They are used in energy storage, filtering, subbing, coupling and decoupling, sensing, and high-power pulsing. With such a versatile range of applications, all having unique needs, capacitors come in many different sizes and designs. Power range, operating temperature, efficiency needs, or reliability concerns will play a large role in capacitor selection. Embedding of capacitors enhances the performance of capacitors further, while also improving the form-factor and efficiency. While capacitor embedding has primarily been delegated to high-frequency filtering, a second wave of embedding, both for energy storage and decoupling purposes, is arising from advances in nanostructured materials, design and processes. This section of the report will review the state-of-the-art capacitor technologies and recent advances that are pushing towards a new era of packaging for high-performance 3D systems. The needs that are driving research and development will be identified. Both ongoing and emerging trends will be analyzed. Predictions for the future will be made.

Excerpt from Embedded Capacitors Section

As we discussed, there is a trend towards capacitor embedding driven by system miniaturization and performance benefits. Companies have made great strides towards this end, with on-chip and on-package decoupling becoming more and more commonplace. Already, on-chip filtering is frequently used. With some capacitor technologies, such as laminates, the technology has been around for a while but limited to low-capacitance requirements that are typically seen in bypass capacitors. In other cases, such as with ceramic and silicon capacitors, wide-spread commercialization of the embedded technology for decoupling applications has arisen due to market needs in high-performance computing and application processors and will only continue to grow. Finally, in some cases, as with electrolytic capacitors, opportunities exist but the art is still largely developmental. Figure 0-1 summarizes the evolution of capacitors to the point of embedding and what technological advances enable the continued development.

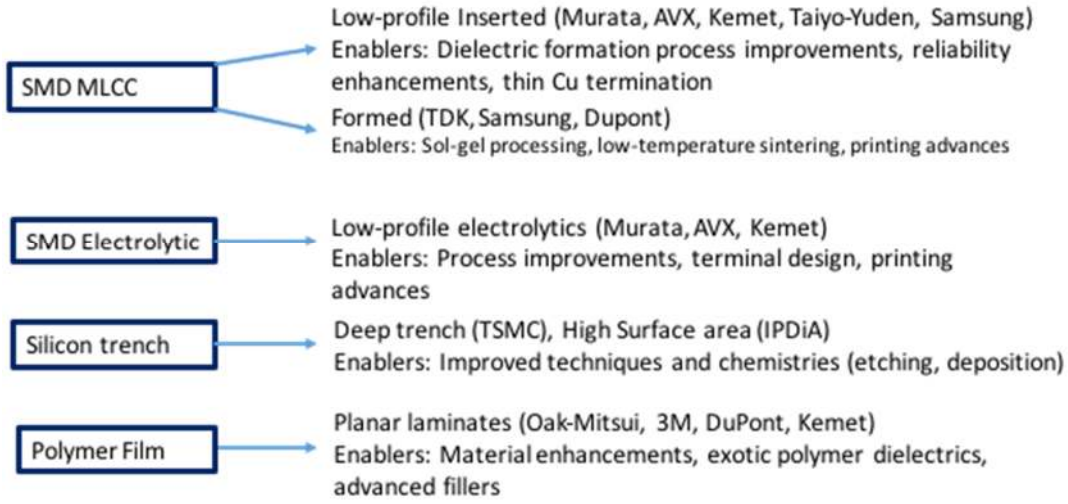


Figure 0-1. Evolution of capacitor technologies from surface-mounted devices to embedded devices with key manufacturers (Source: Georgia Institute of Technology)

There are many ways in which a capacitor can be integrated into a package. The most standard implementation is surface-mounting onto the package substrate. In this approach, the passives are mounted to the side of the IC. These are referred to as “die-side capacitors”. Instead of routing the connection through the substrate and board, the length can be reduced by simply routing through the substrate. For example, Ni base-metal electrode MLCCs for decoupling are used in almost all silicon-based processor packages. The next step of evolution is placing components on the backside of the substrate, referred to as “land-side” capacitors. However, the routing distance through the package-to-surface-mounted devices (SMDs) is still much longer than routing to capacitors embedded within the substrate directly beneath the IC. For this to occur, the capacitor can be laminated into a core material, forming a capacitor-embedded functional substrate. Figure 0-2 summarizes the different ways passives can be integrated into the package [14, 15]. Manufacturers should consider cost versus performance trade-offs as component-embedding can sometimes be more expensive than the component itself.

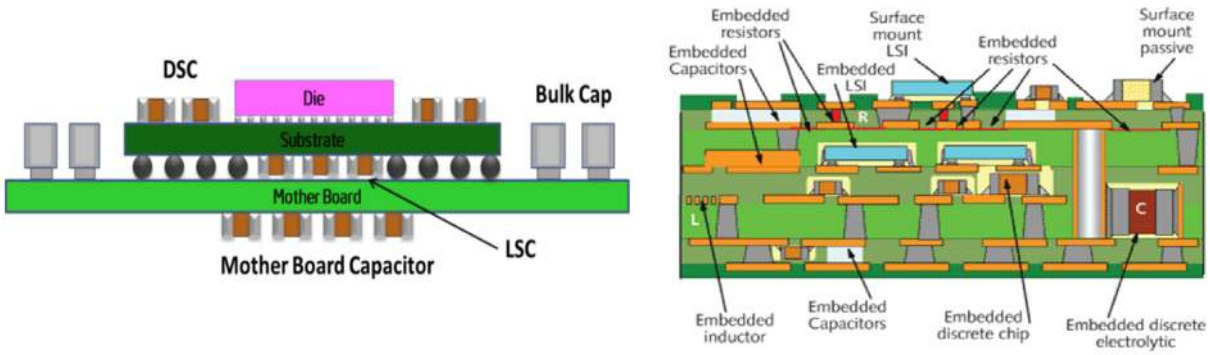


Figure 0-2. (a) Mounted capacitors in a typical board-system (Source: [15]) (b) Efficient integration of passives in a functional substrate (Source: [14])

Laminates

Embedded laminate capacitors find use in mainly high-frequency filtering and noise reduction, and due to their ultra-low loss and planar designs, can be found in many high-performance 3D systems. For power applications, their use is limited due to their small capacitance values. However, as laminate materials continue to improve, the capacitance densities are improving somewhat. The most common way companies have done this is by adding ferroelectric fillers to the laminates to increase the dielectric constant. In the early 2000's Motorola developed a photo dielectric with a permittivity of 20-22 using this concept [16]. In another example, 3M has an embeddable laminate capacitor with copper thickness down to 6 µm that can achieve up to 6.2 nF/cm^2 (Figure 0-3) [17]. The permittivity D_k is achieved using $BaTiO_3$-based particle fillers.

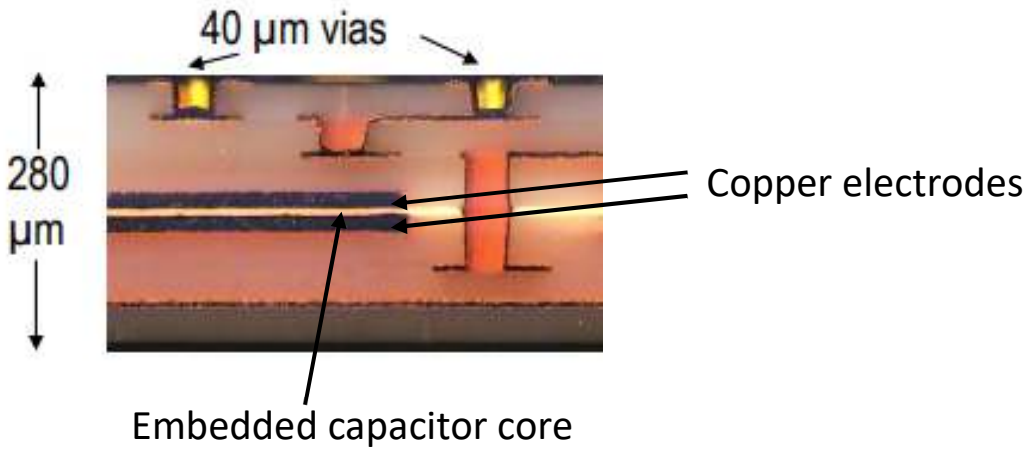


Figure 0-3. C-Ply high-permittivity laminate from 3M embedded in substrate (Source: [17])

Oak-Mitsui similarly used lamination of polymer-ceramic composite films onto copper foil, followed by subtractive patterning and metallization to get embedded capacitor arrays. They can achieve a slightly higher permittivity at the expense of dielectric thickness, so the capacitance is still limited to 1.7 nF/cm^2. Some of the properties for Oak-Mitsui's FaradFlex are listed in Table 0-1 [18].

Properties	Test Method	MC12TM	MC8TM	MC16T	MC25ST	MC25LD
Dielectric Thickness, µm	IPC or others	12	8	16	25	25
Cp @1 MHz, nF/in^2(pF/cm^2)	Nominal	4.2 (650)	7.1 (1100)	11 (1700)	4.3 (660)	2.1 (320)
Dk (Dielectric Constant) @ 1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	10.0/ 9.5	10.5/ 10.0	30.0/ 25,0	18.5/ 18.0	8.3/ 7.8
Df (Loss Tangent) @ 1 MHz/ 1 GHz	IPC TM-650 2.5.5.2	0.015/ 0.020	0.020/ 0.021	0.034/ 0.036	0.004/ 0.008	0.0027/ 0.0032
Peel Strength, lbs/ linear in.	IPC TM-650 2.5.5.2	5	5	5	4	4
Dielectric Strength, kV/mil	IPC TM-650 2.4.9	5	4	2	2	2

Table 0-1. Properties of FaradFlex laminate film (Source: [18])

While laminate composites do a good job of achieving low-impedance filtering and high stability, the capacitance is clearly still limited. As soon as the polymer matrix is added to the ceramic particles, the ε_r goes from >100 down to <30, limiting the use for energy storage applications. Therefore, research has turned to other capacitor technologies to reach higher capacitance values from the substrate.

Inserted MLCCs

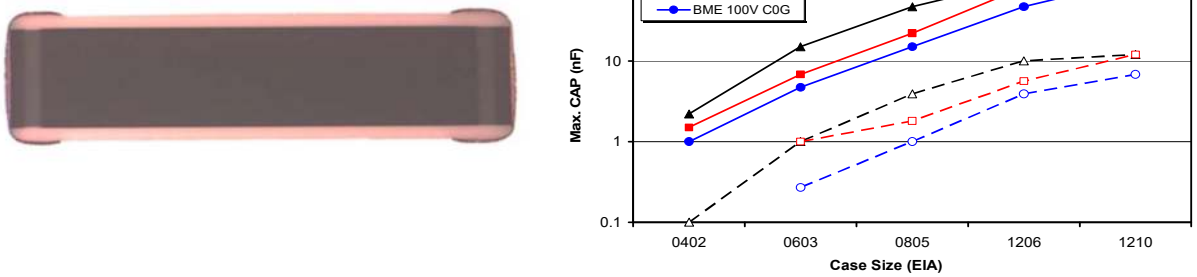
Smaller footprints and thinner form factors are needed to accommodate miniaturized, fine-grain power management with ultra-short interconnection lengths. Overall, MLCC demand has continued to increase, and part of that is due to their encroachment on other capacitor technology markets such as tantalum. Demand for smaller case sizes, especially 0402 and 0201, have been the main contributors to that growth [19]. Traditionally utilized as surface-mounted devices (SMDs), discrete MLCCs are becoming so thin that embedding within the package is possible. There are some key technologies that have enabled this development to the point of commercial manufacturing.

Termination Design

Precious-metal inner electrodes (PMEs) such as Pd-Au or Ag were used for a long time due to their processability with ceramic dielectrics. However, base-metal electrode (BME) BME MLCCs based on Ni inner electrodes were developed in the 1990's with a similar reliability to PME MLCC.

This development was driven by Japanese manufacturers' Taiyo Yuden, Murata & TDK because the high cost of palladium made their MLCC uncompetitive. Other manufacturers such as Samsung, KEMET and AVX adopted this technology to MLCCs based on barium titanite dielectrics. KEMET has pioneered the development of paraelectric dielectrics using Ni (as documented later in this section). Thinner layer MLCC technologies with high CV at lower voltage ratings for consumer electronics have been exclusively developed with Ni BME technology, making this, by far, the most common capacitor type by volume and market share. The use of PME capacitors in some MLCC applications that require large case size and high voltage continues but is cost-prohibitive and being challenged by thinner-layer, higher-capacitance Ni BME MLCCs. Copper inner electrodes have also been commercialized for high-frequency RF capacitors to achieve high Q, but this remains a relatively small specialty market.

Another benefit of using BMEs is the compatibility with $CaZrO_3$ dielectrics. A class I dielectric, $CaZrO_3$ has an improved dielectric strength compared to the class I dielectric traditionally used with PMEs, $BaNdTiO_3$ (BNT). This enables thinner dielectric layers and improved density. Figure 0-4 shows the thin dielectric layers and improved capacitance values using BMEs versus PMEs [20].



(a) (b)

Figure 0-4. (a) Hundreds of thin electrode-dielectric layers in BME-based C0G capacitor [21] (b) Improved density resulting from BME and CaZrO3 dielectric [20]

However, using a Ni inner electrode instead of a PME necessitates chemistry changes in the dielectric itself (in the form of an increased ratio of Barium to Titanium) so that there is more resistance to reduction during cofiring. Those changes often lead to quicker wear-out as insulation resistance degrades faster. The reduced insulation resistance is related to oxygen vacancies, and will be further discussed in the section, "Technology Roadblock and Solutions." Therefore, well-defined sintering processes are needed to prevent electrode oxidation and minimize defects in the dielectric.

Changes have also been applied to the terminal architecture to provide improved impedance characteristics. Lower ESL is especially important for high-frequency decoupling, as components move closer to the IC and a push to high bandwidth processing continues. One development in capacitor terminal design is the reverse terminal option. By designing the capacitor so that the terminals fall on the longer side, the terminals are moved closer together and the inductance loop is reduced (Figure 0-5). Many companies are now offering flipped-terminal options, including Samsung, TDK, and Murata.

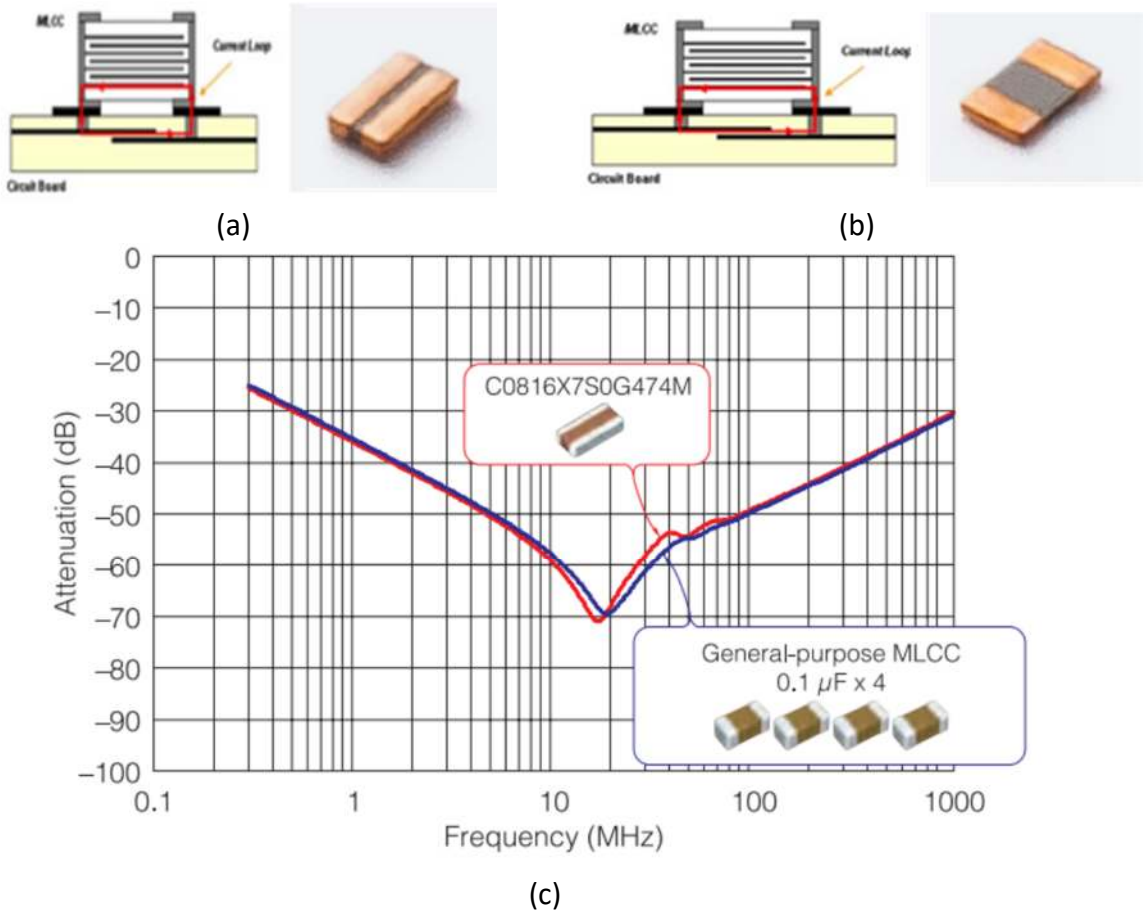
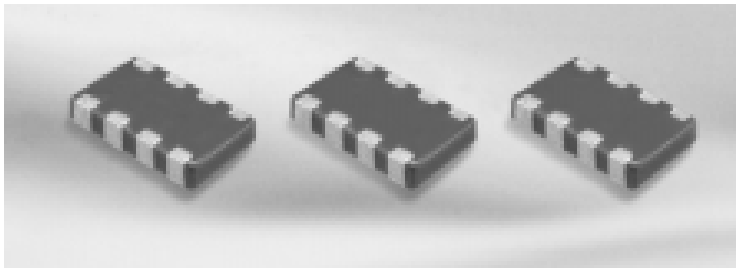
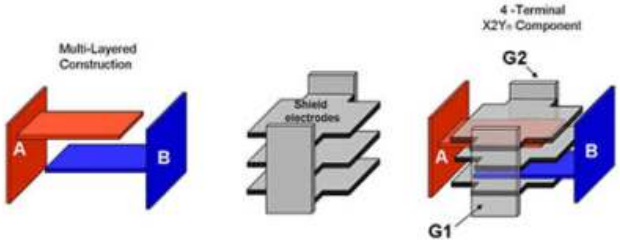


Figure 0-5. Capacitor inductance loop using (a) flipped-terminal design versus (b) standard terminal design (Source: Samsung) (c) Flipped terminal design with similar frequency characteristics as four standard MLCCs in parallel (Source: TDK)

Another method of ESL reduction is by EMI shielding (Figure 0-6). Extra shield electrodes can be added to surround the power and ground electrode layers. Cancellation of mutual inductance is achieved by the alternating flow of current in the shielding layers. The result is a reduced ESL and loss, improving the high-frequency capabilities of the capacitors.



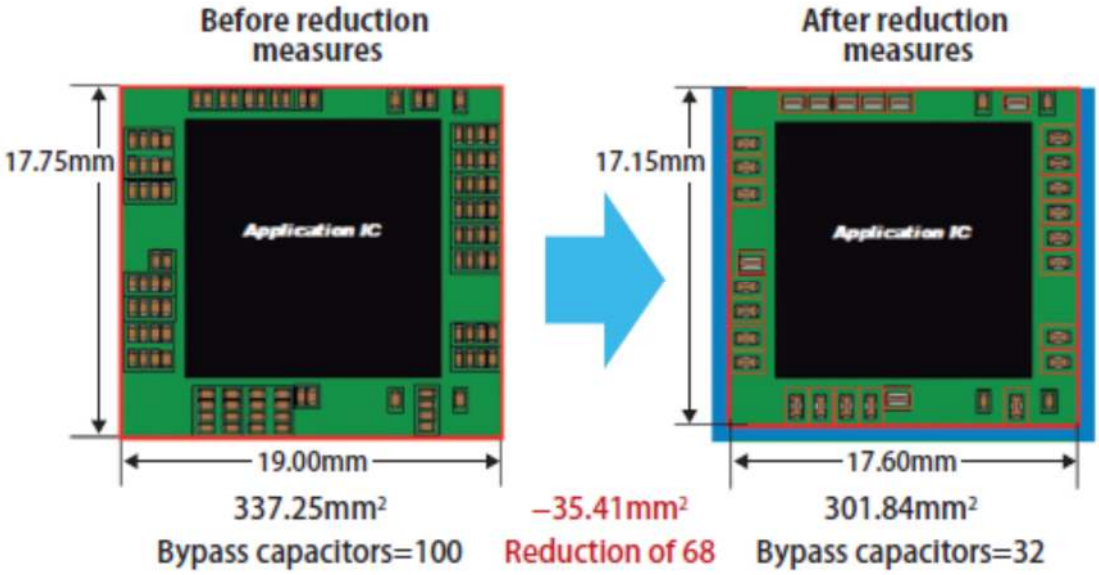
(a)



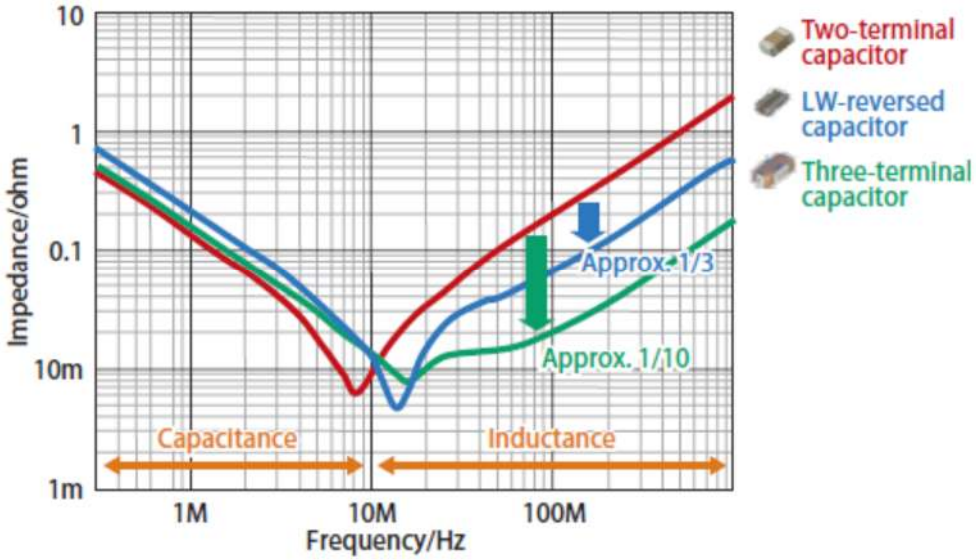
(b)

Figure 0-6. (a) Multi-terminal EMI-suppressed MLCCs with (b) internal shielding electrodes (Source: Samsung)

Usually when decoupling high-frequency processors, many capacitors in parallel are needed to reduce the total impedance of the capacitor and interconnections. With multiple terminals accessing the electrode layers, the internal inductance current can be distributed across so that they are effectively inductors in parallel, thereby reducing the total ESL. Murata has implemented this idea into their discrete components (Figure 0-7). Since not as many capacitors in parallel are needed, the total number of on-board decoupling capacitors is reduced. Only ~25 % or less of the original number of decoupling capacitors are needed, depending on the decoupling frequency, resulting in huge footprint savings and reduced board space. This becomes even more critical as efforts to remove the circuit board all together continue.



(a)



(b)

Figure 0-7. (a) Board space savings resulting from the reduction in number of decoupling capacitors when using low ESL, multi-terminal designs (a) Reduced impedance from non-standard terminal designs (Source: Murata)

Capacitor References

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Excerpts from INDUCTORS Chapter

Excerpt from Introduction

Increased power densities and functionality in today's electronic system drives the need to miniaturize power modules and integrate them close to the loads (ex. Processors) for efficient power management. Power modules consist of active components such as switches, drivers and controllers and passives components such as inductors. Package integration, so far, focused on embedding active components to realize the miniaturization of power modules. However, the module size is still controlled by the bulky inductors, which occupy a large footprint and thickness on the board. To realize true miniaturization of power modules, the inductors need to be miniaturized and integrated within the substrates. Integrated inductors allow them to be in proximity to ICs, resulting in short power delivery length and low parasitics. This will eventually increase the efficiency of the power modules.

There are two ways to integrate inductors with substrates. One way is to fabricate inductors separately as discrete inductors and then insert them into the substrates. These inductors are referred as "inserted inductors" in this report. The other way to integrate inductors into substrates is to directly fabricate them as films in the substrates. These inductors are called "formed inductors" in this report. The inserted and formed inductors embedded in the package substrates are shown in Figure 0-1. For both types of inductors, suitable inductor structures and advance in magnetic materials are the key factors to realize size reduction and integration of inductors with substrates.

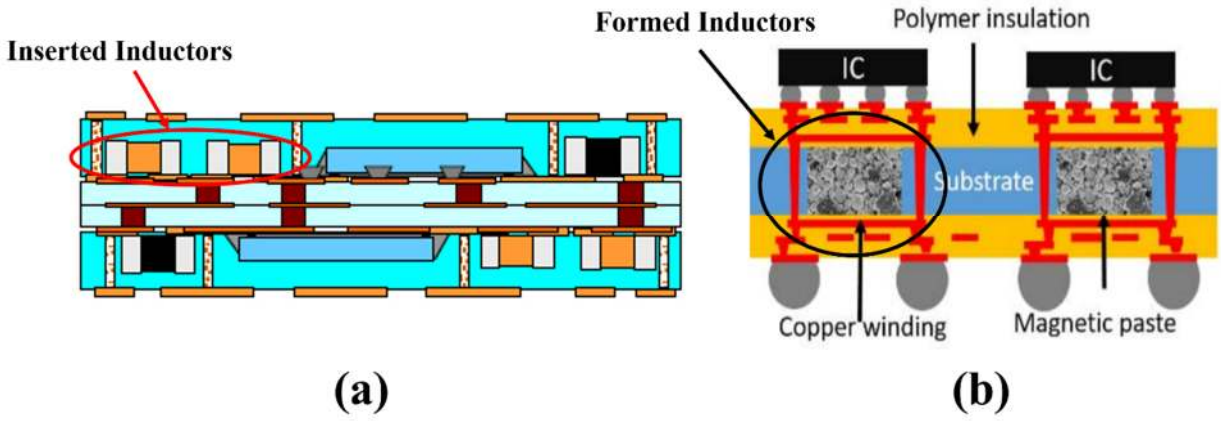

Figure 0-1: Cross-section of substrates with (a) inserted inductors (b) formed inductors [1, 2]

Excerpt from Formed Inductors Section

In addition to insert discrete inductors into substrates, inductors can also be formed directly on substrates. In this section, several formed inductors are discussed. These inductors can be either formed at wafer-level or package-level.

(1) Wafer-integrated Inductors

By using the standard CMOS manufacturing processes, magnetic inductors with small profile can be integrated with CMOS ICs using back-end compatible process options [23]. Ferric, Inc demonstrated magnetic thin-film inductors that are integrated into the ICs, as shown in Figure 0-2. The inductors allow a shorter path for the power to be delivered to the ICs, resulting in a lower I^2R loss. The magnetic materials in the inductors are made of amorphous Cobalt alloy with low coercivity (< 1 Oe) and high saturation field (~ 25 Oe). The magnetic films are separated by thin insulation layers, as shown in Figure 0-3, in order to suppress eddy current loss. The multilayered magnetic films show high permeability of 600 up to 100 MHz. Inductors with the films as magnetic cores show stable inductance until 100 MHz as shown in Figure 0-4 [23].

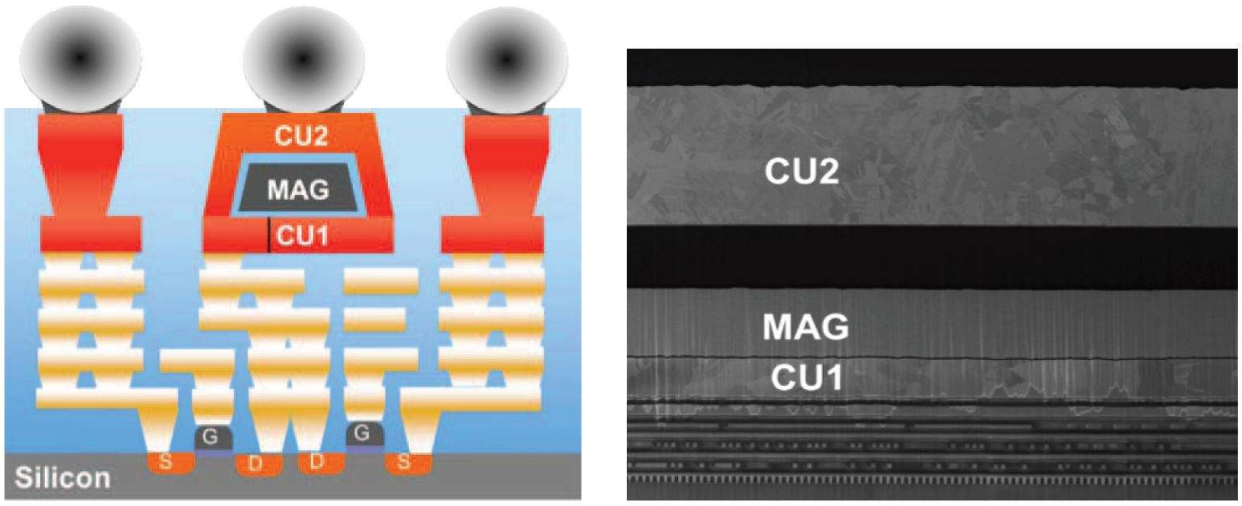

Figure 0-2: Left: Illustration of magnetic thin-film inductors integrated with ICs; Right: SEM cross-section of magnetic thin-film inductors integrated with ICs[23]

Figure 0-3: SEM of multilayered magnetic films[23]

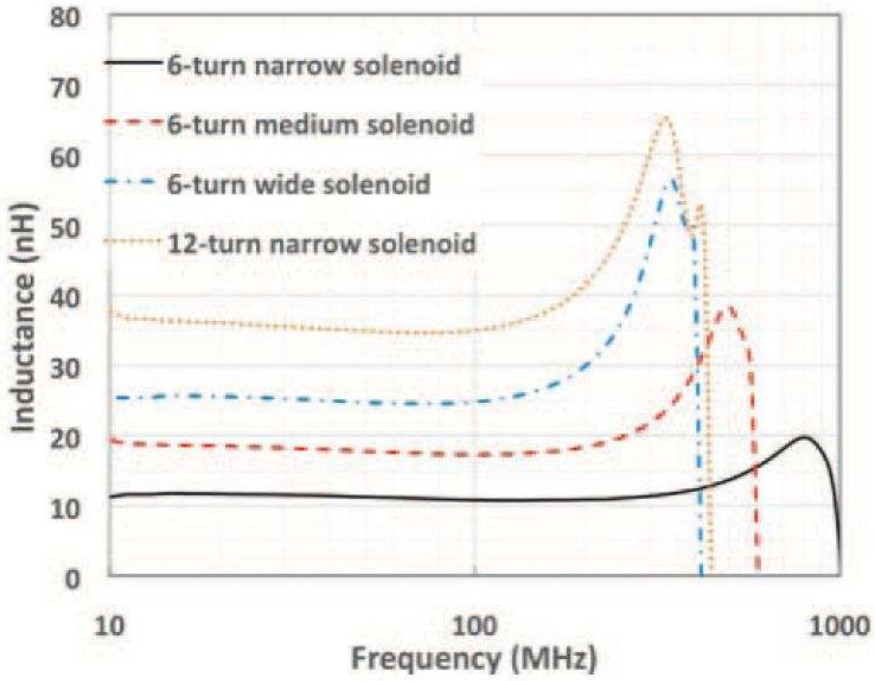

Figure 0-4: Inductance of magnetic thin-film inductors – source [23]

Radial field anisotropy to enhance power handling in toroid inductors:

Because of their high power-handling characteristics, toroidal inductors are good candidates for power applications. For toroidal inductors, all the magnetic flux is constrained within the magnetic cores, forming a closed magnetic loop. The closed loop leads to low flux leakage and high performance. As compared to spiral or stripline inductors, which require deposition of two magnetic layers and vias, toroidal inductors only need one magnetic layer. This

can reduce the cost of the deposition done by expensive and low-throughput processes such as sputtering. Because the magnetic flux changes direction as it travels along the magnetic cores, the cores need to have a radial anisotropy property for high performance. The illustration of the radial anisotropy is shown in Figure 0-5. The Magnetics and Power Electronics Research Group at Dartmouth College has demonstrated a way to induce radial anisotropy to toroidal inductors as shown in Figure 0-6 [24]. The fabrication process is CMOS-compatible and allow the inductors to be integrated onto Si substrates along with the ICs. Fabrication of toroid inductors on Si substrate with induced radial anisotropy is shown in Figure 0-7.

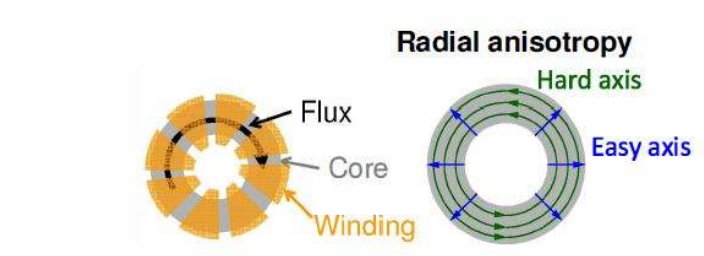

Figure 0-5: Illustration of magnetic flux in toroidal inductors and radial anisotropy [24].

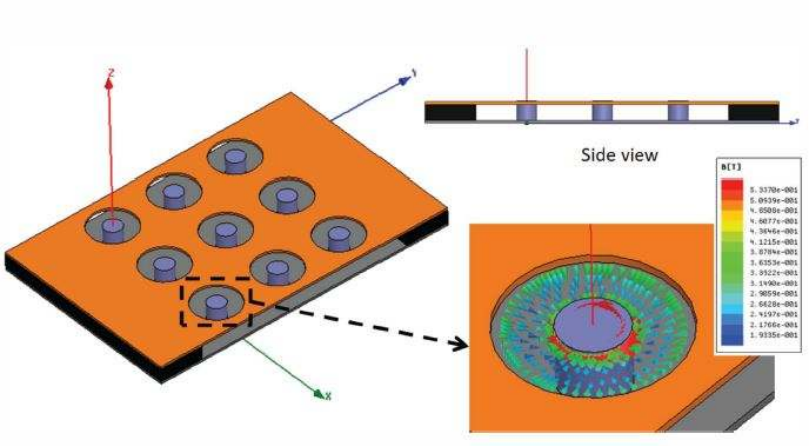

Figure 0-6: Schematic of the structure to introduce radial-anisotropy to toroidal cores – Source [24].

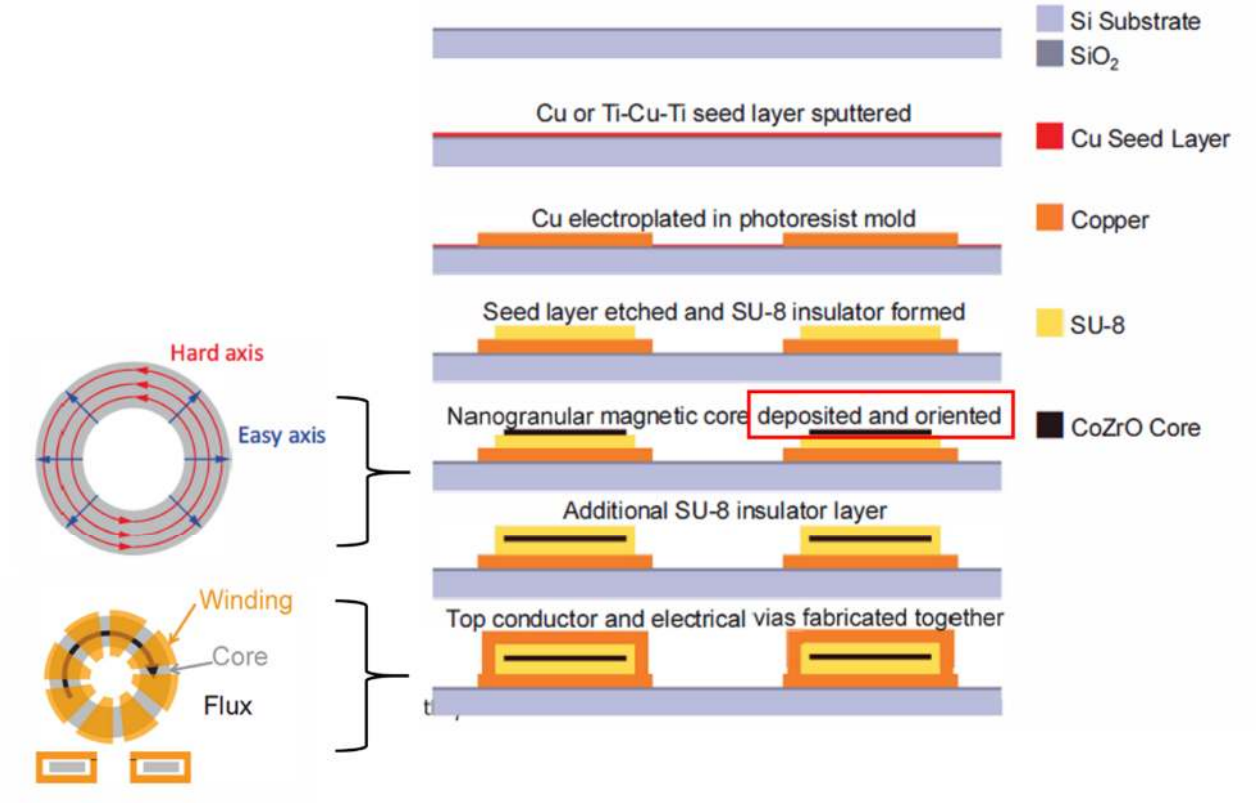

Figure 0-7: Fabrication process of toroid inductors with induced radial anisotropy. The anisotropy is induced by using the structure shown in Figure 0-6.

(2) Package-embedded Inductors

Ferric showed stripline inductors integrated on 500 mm thick flexible substrates as shown in Figure 0-8. Sputtered Co-Zr-Ta-B (CZTB) films were used as the magnetic cores [25, 26]. The films are amorphous to obtain low coercivity (H_c) and high saturation magnetization (M_s). The polyimide substrates are flexible and can be used in wearable electronics. The stripline inductors and flexible polyimide substrates are shown in Figure 0-8. As compared to air-core inductors, the magnetic-core inductors show 2X improvement in inductance. The improved inductance is stable until 1 GHz as shown in Figure 0-9, making them suitable for high-frequency applications. It is worth to note that the inductance variation is less than 5% with 8^o of bending. This stable inductance leads them to applications in flexible electronics.

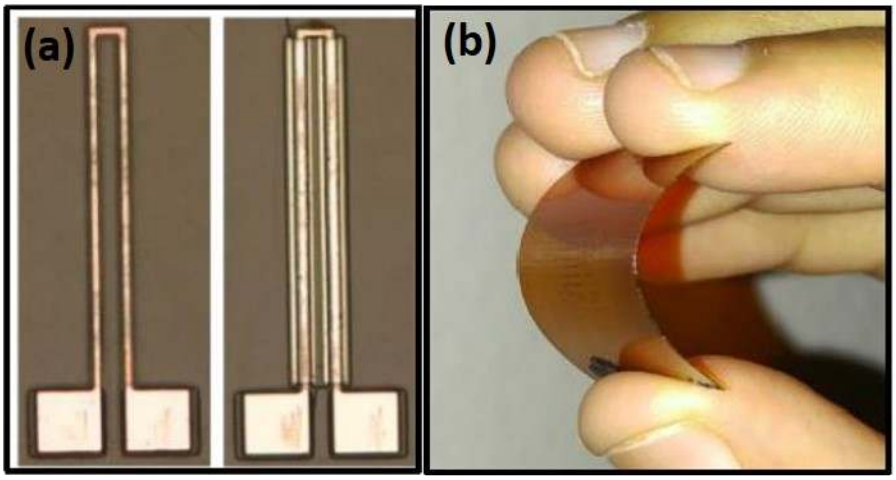

Figure 0-8:(a) Air-core stripline inductors on the left and magnetic-core stripline inductors on the right. (b) flexible polyimide substrates - source [25]

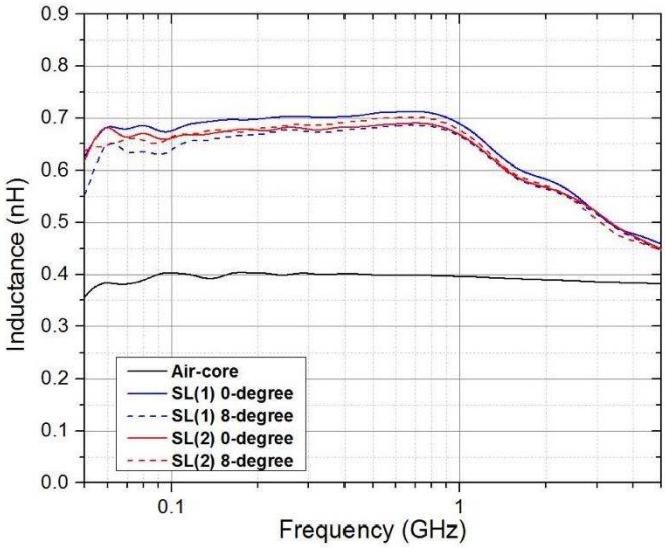

Figure 0-9: Inductance of the air-core inductors, magnetic-core inductors and bended magnetic-core inductors – source [25]

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Excerpt from RESISTORS Chapter

Except from Introduction

The need for miniaturized electronics have increased the global consumption of thin-film resistors by 8% in the last decade, while the cost of these units have steadily decreased over time with an average unit price of $0.082 per unit in 2016 [2]. This highly competitive and aggressive market needs are governed by different application areas, ranging from consumer electronics such as DC/DC convertors, automotive to specialty markets such as medical, defense and oil & gas industry.

The drivers for the resistors include tight tolerances, the corrosion resistance, moisture resistance and rugged nature of the thin-film designs. Paumanok market analysis estimates that the automotive industry is the largest segment in the market for thin-film resistors with almost 15% increased demand in last decade. Automotive industry requires resistors with high precision resistance, high temperature tolerance and anti-sulfur and corrosion resistance. With the increased complexity and density of electronics design, embedding components offers a practical solution to several issues. Embedding can help reduce the size of the package and improve performance. Resistors can be embedded into PCBs as films, using substrate-compatible panel-scale processes, either by the use of prefabricated special layers that are laminated, etched, connected and optionally buried in a multilayer PCBs, or by employing carbon screen-printing. This section of the report briefly discusses the embedded resistor technologies with details on latest commercial products with advanced materials and designs. Novel resistive materials research, with high potential of commercialization in near future, are also reported towards the later part of the report.

Excerpt from Advances in Embedded Resistors Section

A major thrust towards thin-film resistors is also been seen because of its ability to be integrated in the package either as formed or inserted. When the resistor is fabricated directly on the package substrate or wafer, it is termed as a “formed resistor”. On the other hand, if the resistor possesses thin profile such as (01005 or 0201 type), and can be embedded between the substrate layers, it is termed as “inserted resistor”. References [5] and [6] show examples of the formed and inserted resistors respectively.

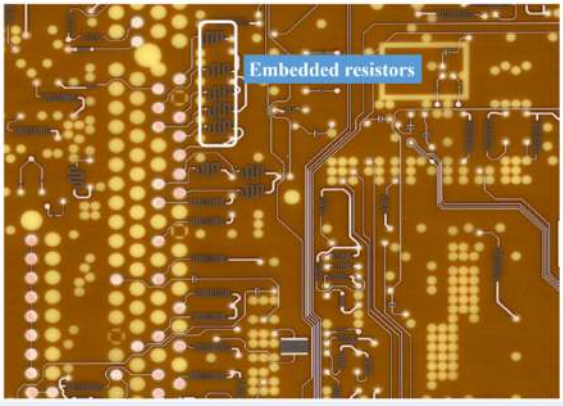

Figure 0-1: Formed resistors on printed circuit board – source Ohmega Technologies, Inc. [5]

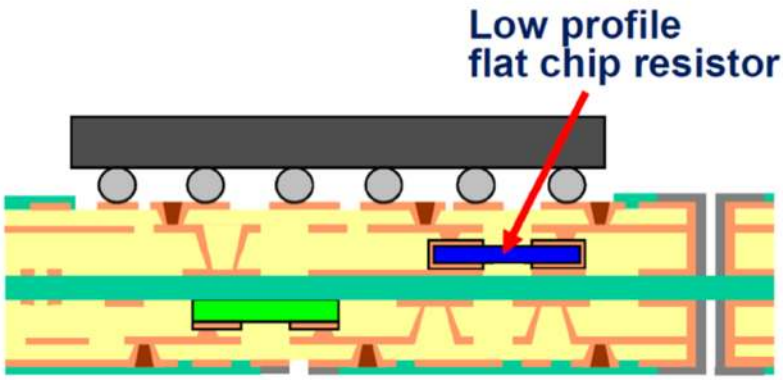

Figure 0-2: Inserted resistors in printed circuit board – source KOA Speer Electronics Inc. [6]

Ticer Technologies

Ticer has designed a low-loss formed resistor ("TCR™" series) for high-frequency applications. Manufactured using a thin-film vapor disposition, TCR ensures the best uniformity of resistor material (NiCr thin-film) across the sheet for higher yields and improved resistor tolerances in multilayer organic packages. It claims to reduce form factor, increase the space available for active components, reduce weight and improve performance. Used with existing printed circuit fabrication processes and chemistries, "TCR™" would minimize or eliminate additional equipment needs and shortens learning curves.

Thickness of the resistive layer is precisely controlled by utilizing a proven vacuum metallization process, which ensures uniform ratios of the elements in the deposited alloy and results in minimal resistance variation. The resistance is isotropic and is not dependent on the machine or grained direction of the copper foil or resistive layer.

Recent commercial resistors with advanced properties are reported next.

Aeroflex

Aeroflex A3RS91.1 PPC and NPC series power resistors show high power in 100 Watts range. Because of the use of substrates with high thermal conductivity, such as aluminum nitride (AlN) and Beryllium oxide (BeO), the resistors provide high power dissipation when mounted on an appropriate heat sink. Figure 0-3 shows conductivity of various ceramic materials. The thermal conductivity of AlN and BeO is much higher than Al_2O_3, which is commonly used as the substrate for resistors. The thickness of the high-power resistors ranges from 0.25 to 1.02 mm. The small thickness shows the potential for substrate-embedding. The resistance of the high-power resistors is only 50 or 100 Ω. Figure 0-4 shows the image of the high-power resistors in different package sizes.

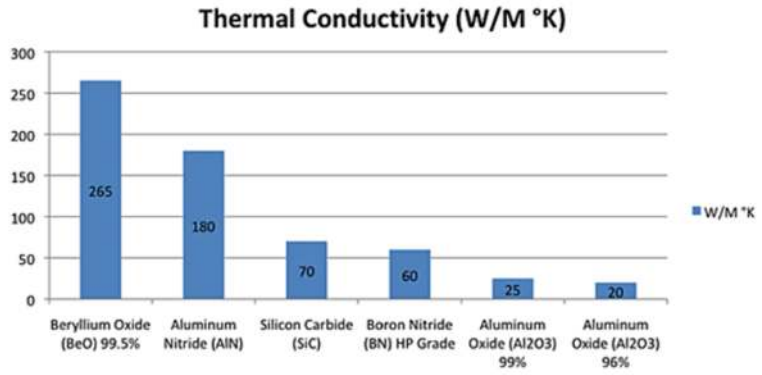

Figure 0-3: Thermal conductivity of various ceramic materials [7].

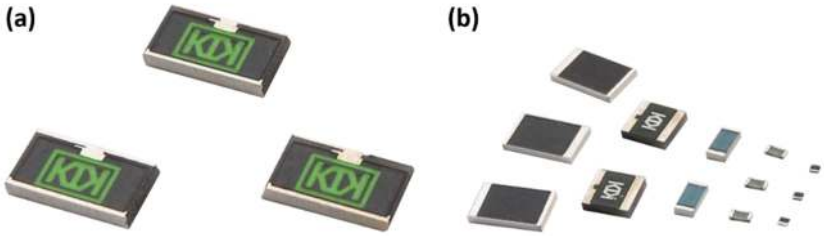

Figure 0-4: Aeroflex high-power resistors (a) AIN substrates (b) BeO substrates – source Aeroflex

Vishay

Vishay RCP series thick-film resistors can handle power of up to 22 Watts because of the use of AIN substrates. The power resistors have wide range of resistances, ranging from 10Ω to 2kΩ and small thickness of 0.51 mm, which make them suitable for substrate embedding. Table 0-1 tabulates the electrical specifications of RCP series resistors;

Table 0-1: Standard electrical specifications of RCP series thick film resistors – source Vishay

Number	Case size	Power rating (standard board mount) W	Power rating (active temperature control) W	Resistance range (Ω)	Tolerance (%)	Temperature coefficient (ppm/^{o}C)
RCP0505	0505	1.4	5.0	10 to 2K	1,2,5	150
RCP0603	0603	1.5	3.9	10 to 2K	1,2,5	150
RCP1206	1206	2.4	11	10 to 2K	1,2,5	150
RCP2512	2512	3.5	22	10 to 2K	1,2,5	150

Vishay
High Power, 1.5kW Discrete Resistors

In 2017, Vishay introduced a 1,500W range of all-welded wire-wound resistors called RBSF1500, which spans 0.234 to 303Ω and offer tolerances down to 1%. These are available as silicon-coated or glass-coated variant as RBEF1500. They are 508mm long and 63.5mm in diameter as shown in Figure 0-5 and weigh 1.9kg each.

Figure 0-5: Photo image of Vishay's high power resistors - Source: Electronics Weekly, Oct 2017

KOA Speer

KOA's XR73 series resistors are especially designed for inserted resistors. The resistors have ultra-low thickness profile of 0.13 and 0.14 mm, which enable the resistors to be embedded into substrates. The resistors also have copper terminations, which assists the formation of reliable copper interconnections. Figure 0-6 shows the process to embed the low-profile resistors into substrates with copper interconnections. By embedding the resistors into substrates, the resistors can be also be shielded from oxidation and corrosive environments resulting in high reliability as illustrated in Figure 0-7[6].

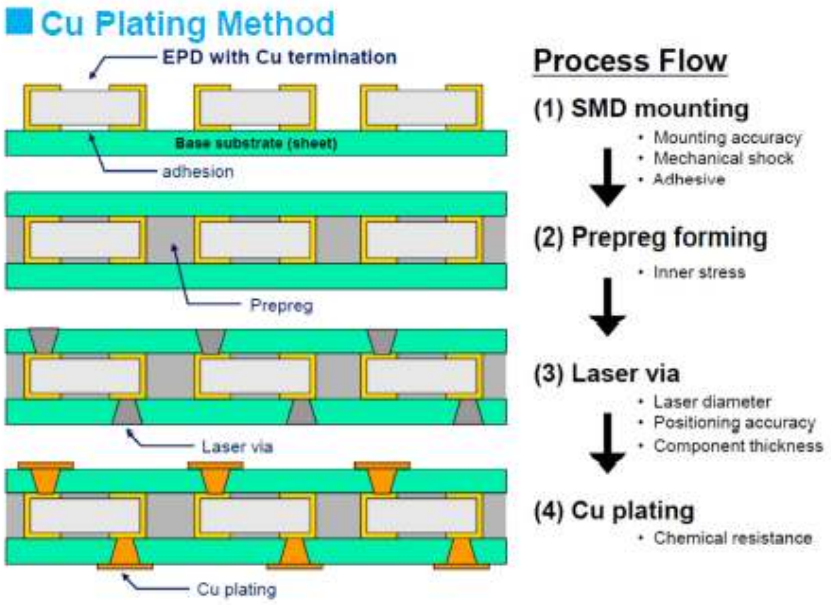

Figure 0-6: Process to embed resistors in substrates – source KOA Speer Electronics Inc. [6]

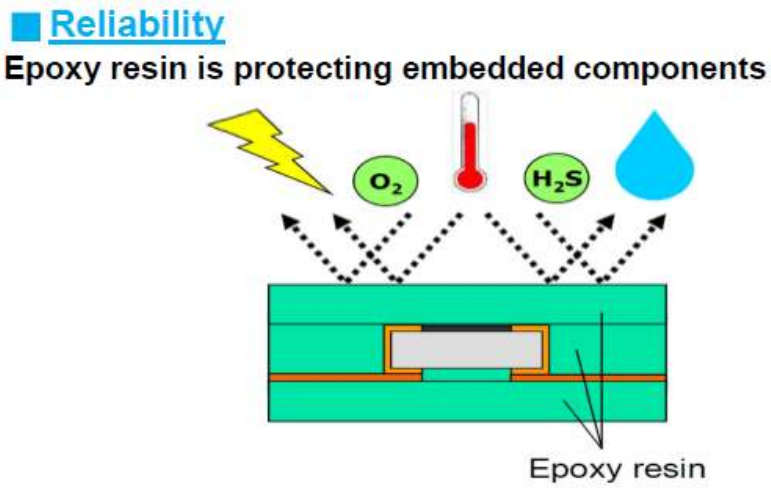

Figure 0-7: Embedded resistors are isolated from corrosion and oxidation environments resulting in high reliability – source KOA Speer Electronics [6].

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Excerpt from 3D Power Packaging with Focus on Embedded Components Chapter

Excerpt from Introduction

As the power semiconductor technology has made impressive progress over the last few decades, power packaging also has advanced in various forms to support different power products [1]. The advances in power module technologies are primarily driven by power system-on-chip (SoC) with wafer-scale integration, or power system-in-package (SiP) with 2D and 3D power packaging in order to achieve the heterogeneous integration of different functional components. Figure 0-1 illustrates a map that defines the terms used in different power products with different functional components [2]. The term "heterogeneous" in this report is refers to any combination of two or more of the different functional components in the middle of Figure 0-1. For example, the high-power multi-chip module in Figure 6-1, is a heterogeneous package form that includes power FETs and power diodes that often appear in a half-bridge configuration, especially in high-power (> 1kW) inverter applications. High-power multi-chip modules may or may not include the control IC and FET drive in the package.

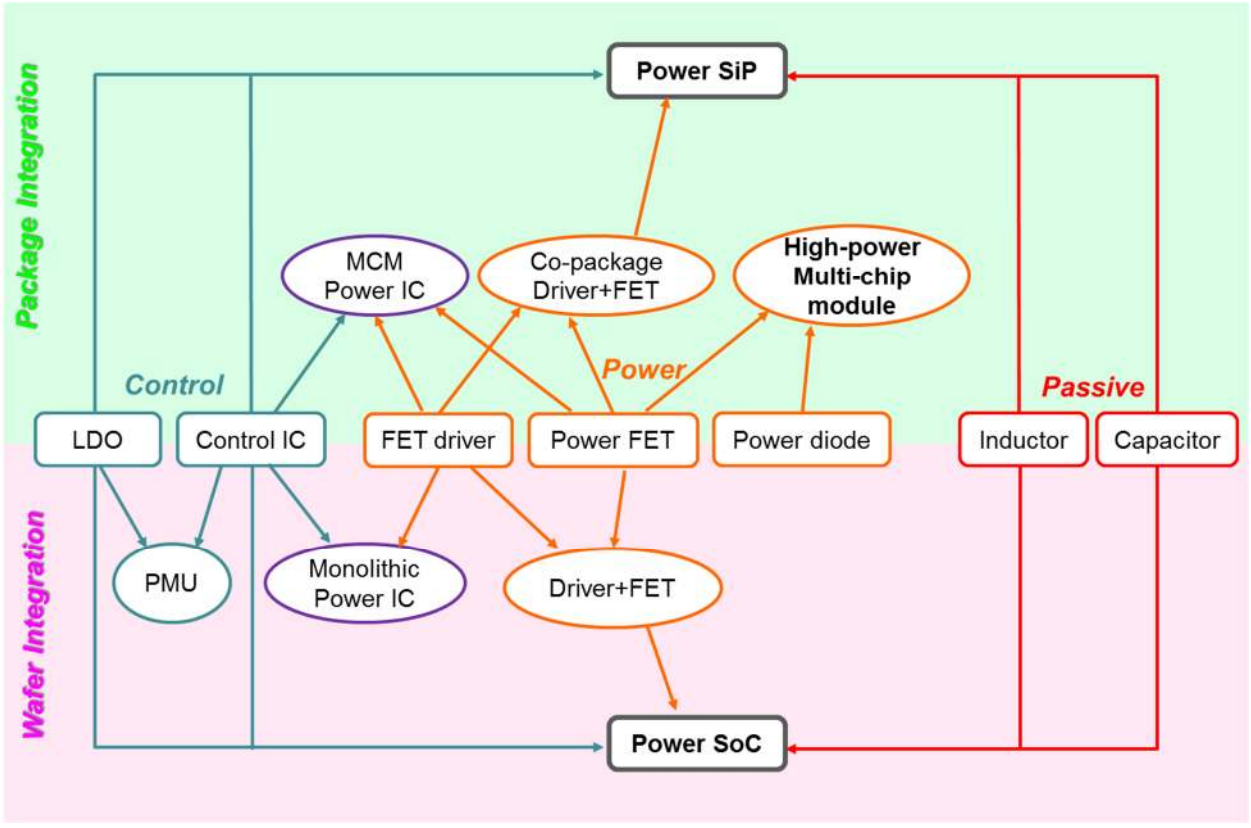

Figure 0-1 Definitions of different power products including power SiP and power SoC [2]

3D power packaging extends the SiP by further utilizing the Z-axis for integration of active- or passive-embedding with vertical interconnects to increase the power density, reduce the package footprint and also lower the cost and packaging layers and interfaces [2].

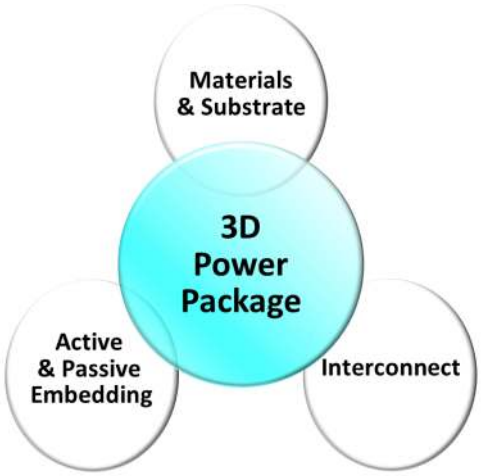

Figure 0-2 Three basic building blocks of 3D power package

Figure 0-2 illustrates the basic building blocks of a 3D power package. This report reviews advances in all the aspects of the three basic building blocks: materials & substrate, interconnect, and active & passive embedding. This section specifically focuses on 3D power packaging with active and passive embedding, while the other two building blocks (substrate materials and interconnects) are discussed in separate sections.

Excerpt from3D Power Package Technologies with Focuses on Embedded Components Section

The major role of packaging in power electronics is to provide electrical connection for semiconductor device to the outer circuitry, to mechanically protect the device from the environment, and to dissipate the generated heat effectively for long-term reliability and safe operation. At the same time, power products have been continuously asked to deliver higher power density at lower cost with improved efficiency [3]. 3D power packaging technologies have been showing rapid development and adoption by many of the power products in recent 5 years in order to fulfill the requirements and needs mentioned above. A noticeable development in 3D power packaging is through embedding technology, which will be discussed in detail in later sections.

The importance of embedding technologies arise from the need for heterogeneous and higher level of integration. In the past, power supply products were either provided in a monolithic power system IC, where all the functions of a system are integrated into a single chip package, or discrete components assembled on a substrate in a planar (2D) manner. Increasing cost and complexity of fabrication process of power SoC led the industry to seek for cost-effective and

functionally flexible alternatives, however, with smaller footprint than the discrete approach [1]. As a result, the concept of SiP (System-in-Package) has emerged as an alternative solution for heterogeneous integration. SiP integrates a number of functional ICs and passives enclosed in a single module (package) that fully or mostly functions as an electronic system. Compared to the monolithic IC approach, SiP technology can provide more integration flexibility, faster time-to-market, and lower R&D and product cost in many of the market segments. These advantages of SiP become particularly more important for high-power modules that are used in areas such as automotive, renewable energy, and other industrial applications [1]. Embedding technology is an advanced SiP approach that enables 3D integration which brings benefits to the power package compared to the conventional packaging technologies. Figure 0-3 illustrates the types of embedding technologies and is described in more detail below. [7]

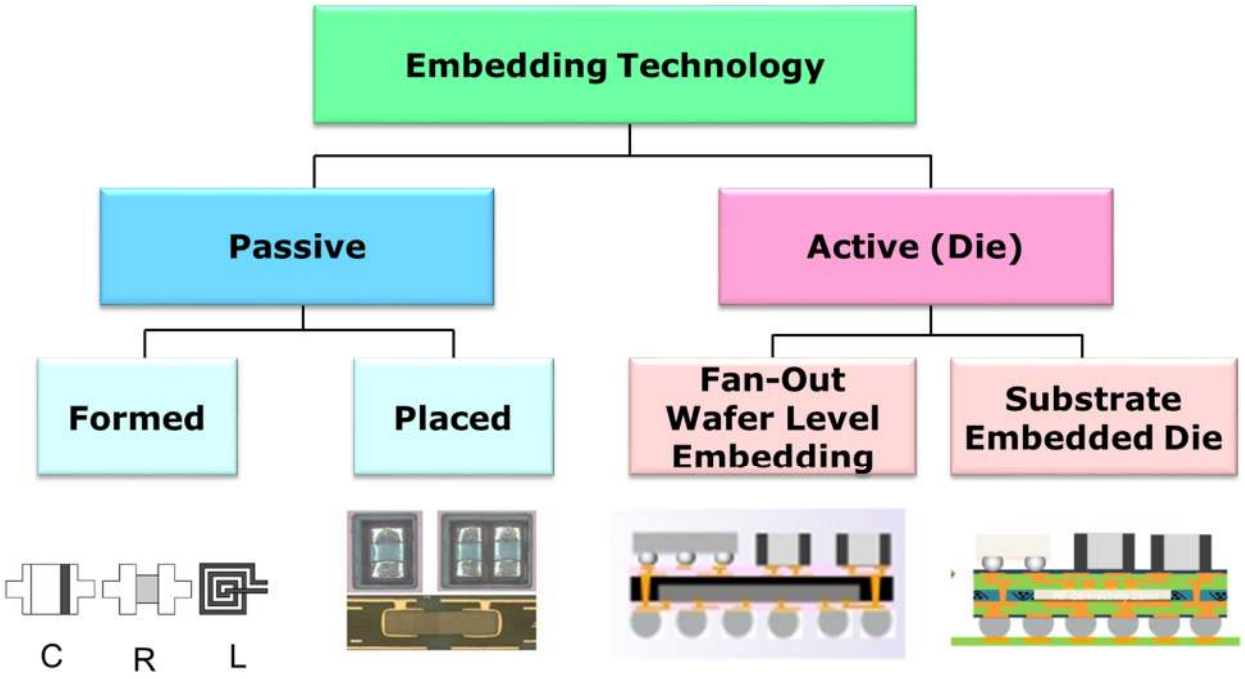

Figure 0-3. Active and passive embedding technologies [7].

Passive components can be embedded into a package by forming method or placing method. These are illustrated in the left side of Figure 0-3. The formed passive elements are created by adding materials to printed circuit structure, whereas the placed passive elements are pre-made discrete components assembled into substrate package during the PCB fabrication process.

Active semiconductor dies such as, control IC, driver, power FET can be embedded through wafer fan-out packaging or panel-substrate embedding methods. In wafer fan-out embedding, dies from a wafer are diced and reconfigured on a wafer-like carrier separated from each other with some distances to allow fan-out of the individual die interconnections. The entire carrier with dies is covered with overmold material, and RDL (redistribution layer) is formed on top of the molding compound after it is cured. The dies are then embedded in a molding compound in a

wafer-level, and becomes individual components after singulation. This type of wafer-level embedding is also called as fan-out wafer level packaging (FOWLP).

Another method of embedding dies is panel-substrate embedding. Substrates can be organic-based such as standard FR4, or inorganic substrates such as glass or ceramic. A typical substrate-embedding process starts with a die placed on a substrate core, and followed by lamination of polymer materials on the top-side. The sandwiched structure, then, goes through sequence of via drilling and filling processes to form RDLs on single or both sides of the die.

The benefits that embedding technology brings to the power products can be summarized as followings:

- Miniaturization through foot-print reduction and higher component integration

- Improved electrical performance by reduced parasitic effects

- Improved mechanical performance through durable Cu interconnections and protective enclosure of package

- Improved thermal performance by direct Cu connections

- Manufacturing cost reduction due to wafer-level or large panel size mass process.

In the following sections, recent examples of both wafer-integration and 3D power packaging technologies will be introduced, and their key innovations related to electrical & thermal performances, and manufacturing will be discussed.

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