Draft Recommended Practice for Electronic Power Subsystems: Parameters, Interfaces, Elements, and Performance

Sponsor

Standards Committee of the IEEE Power Electronics Society

Abstract: This recommended practice provides a technical basis for implementation of electronic power subsystems. It is intended for electronic systems engineers and integrators, electronic power subsystem designers and integrators, as well as power element manufacturers and suppliers. It addresses system-level issues in element or subsystem integration, adaptation, and accommodation. It also defines system-level interface parameters, test methods, and test conditions.

It provides for a systems engineering approach to acquisition, adaptation, and integration of electronic power subsystems, facilitates and promotes a modular approach to element or subsystem integration, and enables effective communication between the end users of power electronics and their manufacturers or suppliers.

Keywords: Adaptation, electronic power distribution, electronic power subsystem, integrators, interaction, logistics, power supply, power electronics, specification, specification language, and system interface.
Introduction

(This is not part of the IEEE Draft Standard P1573, Recommended Practices for Electronic Power Subsystems: Parameters, Interfaces, Elements, and Performance.)

Electronic power subsystems are integral to electronic systems. They perform the tasks of power processing, management, and distribution to all user-level electronics. Clear definition and precise understanding of system-level performance parameters are crucial in building commonalities among different users of electronic power elements. Additionally, system-level understanding of the available electronic power elements or subsystems is the cornerstone to their successful adaptation and integration.

This recommended practice facilitates implementation of electronic power subsystems. It provides specification language at a system-level. It also provides for system-level adaptation and accommodation of commercially available elements or subsystems for specific applications. System-level adaptation and accommodation approaches are provided for use of such elements or subsystems in applications other than those for which they were marketed. This recommended practice is a companion to IEEE Std. 1515-2000 (IEEE Recommended Practice for Electronic Power Subsystems: Parameter Definitions, Test Conditions, and Test Methods). While IEEE Std. 1515-2000 defines the parameters commonly used in specifying power electronic elements, this recommended practice focuses on system-level parameters used to enhance effective element adaptation and integration in developing a subsystem.

This recommended practice provide for a systems engineering approach to acquisition, adaptation, and integration of electronic power subsystems. It facilitates and promotes a modular approach to element or subsystem integration, and enables effective communication between the end users of power electronics and their manufacturers or suppliers. This recommended practice is intended for general users as well as for users for whom performance and logistics are paramount to achieve subsystem availability and affordability.

This recommended practice is intended for use by system engineers, designers, integrators, and manufacturers of power electronic elements. It allows for and promotes effective user-manufacturer cooperation to facilitate element or subsystem specification, acquisition, adaptation, and integration with the performance and logistics predictability and integrity required by today’s demanding applications. It will also be useful for engineers and graduate students who are just entering the field of electronic power systems, since many of the parameters are seldom discussed comprehensively in university courses or in professional educational seminars.
## Participants

The preparation of this recommended practice was accomplished by the IEEE Working Group on Electronic Power Specification (P1573). At the time of its completion, the Working Group (WG) consisted of the following members:

- F. Dong Tan, *Chairman*
- Carlos Gonzalez, *Secretary*

<table>
<thead>
<tr>
<th>Rich Buck</th>
<th>Harry Lamberth</th>
<th>Joe Ortiz</th>
</tr>
</thead>
<tbody>
<tr>
<td>Dave Cooper</td>
<td>Anthony F. Laviano</td>
<td>Ernie Parker</td>
</tr>
<tr>
<td>Rick Eddins</td>
<td>Christian Lazarovici</td>
<td>George Schoneman</td>
</tr>
<tr>
<td>Ernest Fierheller</td>
<td>Yan-Fei Liu</td>
<td>Marvin Soraya</td>
</tr>
<tr>
<td>William A. Hanna</td>
<td>Glen Logan</td>
<td>Wai L. Tam</td>
</tr>
<tr>
<td>George Kaelin</td>
<td>Ed Mabe</td>
<td>Joe Ullman</td>
</tr>
<tr>
<td>Bryan Kellogg</td>
<td>Ken Martindale</td>
<td>Bruce Wright</td>
</tr>
<tr>
<td></td>
<td>Ishaque S. Mehdi</td>
<td></td>
</tr>
</tbody>
</table>

The following members of the balloting committee voted on this standard:
(IEEE to supply)

When the IEEE-SA Standards Board approved this standard on ???, 2002, it had the following membership:
(IEEE to supply)
# Table of Contents

1. Overview .................................................................................................................. 1  
   1.1. Scope .................................................................................................................. 1  
   1.2. Purpose .............................................................................................................. 1  
   1.3. Organization of this recommended practice ...................................................... 1  
2. References ................................................................................................................ 3  
3. Definition of abbreviations, acronyms, and terms ...................................................... 4  
   3.1. Acronyms .......................................................................................................... 4  
   3.2. Terms ................................................................................................................ 6  
      3.2.1. Combined effects ....................................................................................... 6  
      3.2.2. Commercial component ........................................................................... 6  
      3.2.3. Commercial item ..................................................................................... 6  
      3.2.4. Commercial off-the-shelf ......................................................................... 7  
      3.2.5. Cooling medium ....................................................................................... 7  
      3.2.6. Electrical terminations .............................................................................. 7  
      3.2.7. Element ...................................................................................................... 7  
      3.2.8. Input voltage spikes ................................................................................... 7  
      3.2.9. Input voltage transients ............................................................................ 7  
      3.2.10. Logistics ................................................................................................ 7  
      3.2.11. Platform ................................................................................................ 7  
      3.2.12. Power density ......................................................................................... 7  
      3.2.13. Supportability ......................................................................................... 7  
      3.2.14. Synchronization of elements ................................................................... 7  
4. Element-level parameters ......................................................................................... 8  
   4.1. Set point voltage accuracy ................................................................................. 8  
      4.1.1. Definition .................................................................................................. 8  
   4.2. Maximum power dissipation ............................................................................ 8  
      4.2.1. Definition ................................................................................................ 8  
   4.3. Contact resistance ............................................................................................ 8  
      4.3.1. Definition ................................................................................................ 8  
      4.3.2. Test method ............................................................................................. 8  
      4.3.3. Test condition .......................................................................................... 8  
   4.4. Input undervoltage protection ........................................................................ 8  
      4.4.1. Definition ................................................................................................ 8  
      4.4.2. Test method ............................................................................................ 8  
      4.4.3. Test condition ........................................................................................ 8  
   4.5. Input overvoltage protection .......................................................................... 9  
      4.5.1. Definition ................................................................................................ 9  
      4.5.2. Test method ........................................................................................... 9  
      4.5.3. Test conditions ....................................................................................... 10  
   4.6. Overtemperature shutdown ............................................................................ 10  
      4.6.1. Definition ................................................................................................10  
      4.6.2. Test method ............................................................................................10  
      4.6.3. Test condition ........................................................................................11  
   4.7. Reverse voltage protection ......................................................................... 11  
      4.7.1. Definition ...............................................................................................11  

8/19/2002 Copyright ©2002 IEEE. All rights reserved. iii  
This is an unapproved IEEE Standards Draft, subject to change.
4.7.2. Test method (input reverse voltage) .......................................................... 11
4.7.3. Test method (output reverse voltage) ...................................................... 12
4.7.4. Test condition (input reverse voltage) .................................................. 13
4.7.5. Test condition (output reverse voltage) ............................................... 13
4.8. Turn-on time ......................................................................................... 13
4.9. Regulation, combined ............................................................................ 13
  4.9.1. Definition ......................................................................................... 13
  4.9.2. Test method ..................................................................................... 13
  4.9.3. Test condition ................................................................................... 13
4.10. Regulation effects due to aging ............................................................... 13
  4.10.1. Definition ....................................................................................... 13
4.11. Lightning ................................................................................................ 13
  4.11.1. Definition ....................................................................................... 13
4.12. Surge .................................................................................................... 14
  4.12.1. Definition ....................................................................................... 14
4.13. Sag ....................................................................................................... 14
  4.13.1. Definition ....................................................................................... 14
4.14. Transients (spikes) ............................................................................... 14
  4.14.1. Definition ....................................................................................... 14
5. Electronic power subsystems ..................................................................... 15
  5.1. Interface definition ................................................................................ 15
    5.1.1. Electrical interface ................................................................. 16
    5.1.2. Mechanical interface ............................................................ 17
    5.1.3. Environmental interface ........................................................ 17
    5.1.4. System effectiveness interface ............................................. 17
  5.2. Requirements definition ..................................................................... 18
  5.3. Architectural considerations ............................................................... 19
  5.4. System interaction .............................................................................. 25
6. Electrical interface parameters .................................................................. 27
  6.1. Status monitoring ............................................................................... 27
  6.2. Supervisory control .......................................................................... 27
  6.3. Built-in-test ......................................................................................... 27
    6.3.1. Definition ..................................................................................... 27
  6.4. Electromagnetic compatibility/electromagnetic interference .................. 27
    6.4.1. Conducted interference ................................................................ 28
      6.4.1.1. Differential mode interference ............................................ 28
      6.4.1.2. Common mode interference ............................................. 28
      6.4.1.3. Conducted susceptibility .................................................... 28
    6.4.2. Radiated interference .................................................................. 28
      6.4.2.1. Radiated emissions ............................................................ 28
        6.4.2.1.1. Definition .................................................................. 28
        6.4.2.1.2. Test method ............................................................. 28
        6.4.2.1.3. Test conditions ......................................................... 28
      6.4.2.2. Radiated susceptibility ....................................................... 29
        6.4.2.2.1. Definition ................................................................ 29
        6.4.2.2.2. Test method ............................................................. 29
        6.4.2.2.3. Test condition ........................................................... 29
    6.4.3. Electrical noise ............................................................................ 29
    6.4.4. Electrical noise spectrum ......................................................... 30
7. Mechanical interface parameters ............................................................ 32
   7.1. Packaging ......................................................................................... 32
      7.1.1. Component ............................................................................. 32
      7.1.2. Circuit card assembly ............................................................... 32
      7.1.3. Assembly, chassis, enclosure, box, rack .................................... 32
   7.2. Center of gravity ............................................................................ 32
      7.2.1. Definition ................................................................................ 32
      7.2.2. Test method ............................................................................ 33
   7.3. Cooling or thermal energy dissipation process ................................. 33
      7.3.1. Thermal interface ................................................................... 33
         7.3.1.1. Conduction cooling ............................................................. 33
            7.3.1.1.1. Solid physical junction .................................................. 33
            7.3.1.1.2. Convection cooling ....................................................... 33
            7.3.1.1.3. Forced gas or liquid cooling ........................................ 33
         7.3.1.2. Radiation cooling ............................................................... 33
      7.3.2. Temperature rise ...................................................................... 33
      7.3.3. Maximum inlet temperature ....................................................... 34
   7.4. Flow rate ....................................................................................... 34
      7.4.1. Airflow .................................................................................... 34
      7.4.2. Liquid cooling (closed system) .................................................. 34
      7.4.3. Pressure drop/back pressure ..................................................... 34
   7.5. Heat pipe (phase change) ............................................................... 34

8. Environmental interface parameters ................................................... 35
   8.1. Thermal ......................................................................................... 35
   8.2. Resistance to contaminants ............................................................ 35
      8.2.1. Definition ............................................................................... 35
      8.2.2. Test method ............................................................................ 35
      8.2.3. Test condition ......................................................................... 35
   8.3. Sand and dust ................................................................................ 35
      8.3.1. Definition ............................................................................... 35
      8.3.2. Test method ............................................................................ 35
      8.3.3. Test condition ......................................................................... 36
   8.4. Explosive atmosphere ................................................................... 36
      8.4.1. Definition ............................................................................... 36
      8.4.2. Test method ............................................................................ 36
      8.4.3. Test condition ......................................................................... 36
   8.5. Acoustics ....................................................................................... 36
      8.5.1. Acoustic susceptibility ............................................................... 36
         8.5.1.1. Definition ........................................................................... 36
         8.5.1.2. Test method ....................................................................... 37
         8.5.1.3. Test condition ................................................................... 37
      8.5.2. Acoustic emissions/audible noise ............................................. 37
         8.5.2.1. Definition ........................................................................... 37

6.4.4.1. Definition.................................................................................. 30
6.4.4.2. Test method............................................................................. 30
6.4.5. Electrostatic discharge .................................................................. 30
   6.4.5.1. Definition.............................................................................. 30
   6.4.5.2. Test method ........................................................................... 30
   6.4.5.3. Test conditions ...................................................................... 30
8.5.2.2. Test method ................................................................. 37
8.5.2.3. Test condition ........................................................... 37
8.6. Radiation ................................................................. 37
  8.6.1. Total ionizing dose ....................................................... 37
    8.6.1.1. Definition ........................................................... 37
    8.6.1.2. Test method ........................................................ 37
    8.6.1.3. Test conditions ..................................................... 37
  8.6.2. Dose rate ............................................................... 38
    8.6.2.1. Definition ........................................................... 38
    8.6.2.2. Test method ........................................................ 38
    8.6.2.3. Test conditions ..................................................... 38
  8.6.3. Single event effects .................................................... 38
    8.6.3.1. Definition ........................................................... 38
    8.6.3.2. Test method ........................................................ 38
    8.6.3.3. Test conditions ..................................................... 38
  8.6.4. Neutron radiation ...................................................... 38
    8.6.4.1. Definition ........................................................... 38
    8.6.4.2. Test method ........................................................ 39
    8.6.4.3. Test conditions ..................................................... 39

9. System effectiveness interface parameters ......................... 40
  9.1. Qualification requirements ............................................ 40
    9.1.1. Qualification by similarity ....................................... 40
    9.1.2. Qualification by inspection ....................................... 40
    9.1.3. Qualification by demonstration ................................. 40
    9.1.4. Qualification by analysis ......................................... 40
    9.1.5. Qualification by test ............................................... 40
  9.2. Quality assurance ...................................................... 40
    9.2.1. Derating ............................................................. 40
    9.2.2. Component quality ................................................ 40
    9.2.3. Screening ............................................................ 40
  9.3. Acceptance testing ..................................................... 41
    9.3.1. Test equipment calibration and standards .................... 41
  9.4. Compliance information ............................................... 41
  9.5. Logistics ................................................................. 41
    9.5.1. Product life .......................................................... 41
        9.5.1.1. Definition ...................................................... 41
    9.5.2. Physical product life .............................................. 41
        9.5.2.1. Definition ...................................................... 41
        9.5.2.2. Test method .................................................... 41
        9.5.2.3. Test condition ................................................ 42
  9.6. Configuration management .......................................... 42
  9.7. Obsolescence .......................................................... 42
  9.8. Discontinuance ........................................................ 42
  9.9. Production line certification ......................................... 42
  9.10. Warranty ............................................................... 42
10. System integration ...................................................... 43
  10.1. System interaction ................................................... 43
    10.1.1. Source impedance and system stability – dc systems .... 43
11. System adaptation

11.1. Electrical interface adaptations

11.1.1. Input voltage and current

11.1.1.1. Power supply with ac input

11.1.1.2. Power supply with dc input

11.1.1.3. Ac input rectifier and filtering

11.1.1.4. Input induced ripple current

11.1.1.5. Power factor correction

11.1.1.6. Output voltage and current mismatch

11.1.2. Protection

11.1.2.1. Input reverse polarity protection

11.1.2.1.1. Input series connection

11.1.2.1.2. Input parallel connection

11.1.2.2. Input undervoltage protection

11.1.2.3. Input overvoltage protection

11.1.2.4. Input transient suppressors
11.1.1.10. Monitoring and control ......................................................... 66
  11.1.10.1. Monitoring and control of commercial item elements .......... 66
  11.1.10.2. Software implementation ............................................... 66

11.2. Mechanical interface adaptation ............................................. 71
  11.2.1. Structural, structural adhesives, vibration ................................. 72
  11.2.2. Potting ........................................................................... 72
  11.2.3. Secondary packaging .......................................................... 72
  11.2.4. Thermal, thermal adhesives, heat sinks, heat exchangers, heaters and coolers .......................................................... 72
  11.2.5. Extra heat shielding ............................................................. 73
  11.2.6. Directing cooling fluid ........................................................ 73
  11.2.7. Shock damping .................................................................. 73

11.3. Environmental interface adaptation ........................................ 73
  11.3.1. Storage temperature .............................................................. 74
    11.3.1.1. Temperature screening ................................................... 74
  11.3.2. Operating temperature ........................................................ 74
  11.3.3. Thermal shock ................................................................... 75
  11.3.4. Humidity with and without condensing environments ................. 75
  11.3.5. Vibration and shock environments ........................................ 75
    11.3.5.1. High impact environment ............................................... 76
  11.3.6. Resistance to materials ........................................................ 76
    11.3.6.1. Sand and dust ................................................................ 76
11.3.6.2. Altitude

11.3.7. Explosive atmosphere

11.3.8. Combined effects

11.3.9. Radiation environment

   11.3.9.1. Incorporating radiation resistance to total dose ionization
   11.3.9.2. Adaptations for commercial space applications
   11.3.9.3. Adaptations for military (USA) space applications
   11.3.9.4. Adaptations for military (USA) nuclear hardened applications

11.4. System effectiveness interface adaptation

   11.4.1. Reliability and redundancy
   11.4.2. Vendor qualification
   11.4.3. Parts screening
   11.4.4. Product qualification
   11.4.5. Module obsolescence and discontinuance

   11.4.5.1. Obsolescence management strategies
   11.4.5.2. Specifications
   11.4.6. Availability
   11.4.7. Usability
   11.4.8. Installability
   11.4.9. Fault tolerance, single point failures
   11.4.10. Supportability
   11.4.11. Economic

11.5. Adaptation analysis techniques

Annex A. (Informative) Bibliography

Annex B. (Informative) Performance

   B.1. Electrical interface performance
   B.2. Mechanical interface performance
   B.3. Environmental interface performance
   B.4. System effectiveness performance

Annex C. (Informative) Parameter index

Annex D. (Informative) Radiation environments

   D.1. Radiation environmental/definition
   D.2. Definition of Terms

      D.2.1. Inherent hardness
      D.2.2. Radiation hardened
      D.2.3. Ionizing radiation
      D.2.4. Burst radiation
      D.2.5. Dose rate or gamma dot
      D.2.6. Alpha particles
      D.2.7. Gamma radiation
      D.2.8. High-energy particle
      D.2.9. Annealing (post-irradiation effects)
      D.2.10. Total Ionizing Dose (TID)
      D.2.11. Displacement Damage
      D.2.13. Single Event Upset (SEU)
      D.2.14. Single Event Latch-up (SEL)
      D.2.15. Single Event Burnout (SEB)
      D.2.16. Single Event Gate Rupture (SEGR)
D.2.17. Linear Energy Transfer (LET) ................................................................. 106
D.2.18. Radiation Hardness Assurance (RHA) .................................................. 106
D.2.19. Radiation Hardness Assured Capability Limit (RHACL) ...................... 106
D.2.20. Source Control Drawing (SCD) ............................................................ 106
D.3. Radiation environments ............................................................................ 106
D.3.1. Radiation hardness requirements ........................................................... 106
D.3.2. Major radiation environments ............................................................... 107
  D.3.2.1. Total ionizing dose ........................................................................ 107
  D.3.2.2. Transient (dose rate) radiation ......................................................... 107
  D.3.2.3. Single event phenomena .................................................................. 107
  D.3.2.4. Neutron radiation ........................................................................... 108
D.3.3. Radiation damage effects ...................................................................... 108
  D.3.3.1. Displacement damage ..................................................................... 108
  D.3.3.2. Ionization effects ............................................................................ 108
D.3.4. Space and military environments .......................................................... 108
  D.3.4.1. Space environment ......................................................................... 108
  D.3.4.2. Military environment ..................................................................... 109
D.4. Radiation design considerations ............................................................... 109
  D.4.1. Conceptual design ............................................................................. 109
  D.4.2. Engineering development phase ........................................................... 110
    D.4.2.1. Incident radiation environment ..................................................... 110
    D.4.2.2. Radiation evaluation process ......................................................... 110
D.5. Radiation testing ....................................................................................... 112
  D.5.1. Radiation-effects testing .................................................................. 112
  D.5.2. Executing radiation-effects testing ...................................................... 112
    D.5.2.1. Radiation sources and test methods for total dose testing ............... 113
    D.5.2.2. Radiation sources and test methods for neutron testing .................. 113
    D.5.2.3. Radiation sources and test methods for dose rate testing ............... 113
    D.5.2.4. Radiation sources and test methods for see testing ....................... 113
## List of Figures

<table>
<thead>
<tr>
<th>Figure</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Test setup for input undervoltage protection</td>
<td>9</td>
</tr>
<tr>
<td>2</td>
<td>Test setup for input overvoltage protection</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>Test setup for overtemperature shutdown</td>
<td>11</td>
</tr>
<tr>
<td>4</td>
<td>Test setup for normal input polarity connection</td>
<td>12</td>
</tr>
<tr>
<td>5</td>
<td>Test setup for reverse input polarity connection</td>
<td>12</td>
</tr>
<tr>
<td>6</td>
<td>Test setup for reverse output polarity connection</td>
<td>13</td>
</tr>
<tr>
<td>7</td>
<td>Relationship between an element and its interfaces</td>
<td>16</td>
</tr>
<tr>
<td>8</td>
<td>Electrical interface</td>
<td>17</td>
</tr>
<tr>
<td>9</td>
<td>Highly integrated power subsystem</td>
<td>19</td>
</tr>
<tr>
<td>10</td>
<td>Modular power subsystem</td>
<td>20</td>
</tr>
<tr>
<td>11</td>
<td>A typical centralized architecture for electronic power subsystems</td>
<td>22</td>
</tr>
<tr>
<td>12</td>
<td>A typical distributed architecture for electronic power subsystems</td>
<td>22</td>
</tr>
<tr>
<td>13</td>
<td>A typical hybrid architecture for electronic power subsystem</td>
<td>23</td>
</tr>
<tr>
<td>14</td>
<td>Electronic power element interfaces and system adaptation</td>
<td>24</td>
</tr>
<tr>
<td>15</td>
<td>An adaptation example for a telecom power subsystem</td>
<td>25</td>
</tr>
<tr>
<td>16</td>
<td>An illustration of various configurations for radiated EMI/EMC tests</td>
<td>29</td>
</tr>
<tr>
<td>17</td>
<td>Component, CCA, and assembly packaging of electronic power subsystems</td>
<td>32</td>
</tr>
<tr>
<td>18</td>
<td>Calculation of stability capacitor</td>
<td>44</td>
</tr>
<tr>
<td>19</td>
<td>System stability test method</td>
<td>44</td>
</tr>
<tr>
<td>20</td>
<td>Overvoltage transient</td>
<td>63</td>
</tr>
<tr>
<td>21</td>
<td>Window detector boundaries</td>
<td>64</td>
</tr>
<tr>
<td>22</td>
<td>Circuit breaker fault current</td>
<td>65</td>
</tr>
<tr>
<td>23</td>
<td>Overvoltage protection response to overvoltage</td>
<td>66</td>
</tr>
<tr>
<td>24</td>
<td>Commercial Item life cycle trends</td>
<td>82</td>
</tr>
<tr>
<td>D-1</td>
<td>Radiation evaluation process for EEE parts</td>
<td>111</td>
</tr>
</tbody>
</table>
List of Tables

Table 1. Example interface considerations ........................................................................................................... 16
Table 2. Architectural interface adaptations ........................................................................................................ 24
Table 3. ESD test standards/methods for classification of ESDS parts. ................................................................. 30
Table 4. ESD classification ....................................................................................................................................... 31
Table 5. ESD testing ................................................................................................................................................ 31
Table 6. Electrical interface adaptations .............................................................................................................. 55
Table 7. Class A radiated emissions (10 meters) ................................................................................................... 69
Table 8. Class A conducted emissions .................................................................................................................. 69
Table 9. Class B radiated emissions (3 meters) ....................................................................................................... 69
Table 10. Class B conducted emissions ................................................................................................................ 69
Table 11. RE102 radiated emissions (ground based) ............................................................................................. 70
Table 12. CE102 conducted emission (basic curve, all application) ..................................................................... 70
Table 13. CE102 limit relaxation for different source input voltage ........................................................................ 70
Table 14. Mechanical interface adaptations ........................................................................................................ 72
Table 15. Environmental interface adaptations .................................................................................................. 74
Table 16. Required radiation resistance ................................................................................................................ 77
Table 17. System effectiveness interface adaptions ............................................................................................... 79
Table B-1. General electrical interface performance ........................................................................................... 87
Table B-2. Electrical interface: output/load performance ...................................................................................... 88
Table B-3. Electrical interface source performance .............................................................................................. 91
Table B-4. Mechanical interface performance ..................................................................................................... 93
Table B-5. Environmental interface performance ............................................................................................... 95
Table B-6. System effectiveness performance ..................................................................................................... 97
Table C-1. General electrical interface parameters ............................................................................................ 98
Table C-2. Electrical output/load interface parameters ......................................................................................... 99
Table C-3. Electrical source interface parameters ............................................................................................... 100
Table C-4. Mechanical interface parameters ...................................................................................................... 101
Table C-5. Environment interface parameters .................................................................................................... 102
Table C-6. System effectiveness interface parameters .......................................................................................... 103
Table D-1. Radiation hardness assurance categories ............................................................................................ 106
Table D-2. Application current radiation hardness needs ...................................................................................... 107
Table D-3. Types and sources of radiation for military applications .................................................................... 109
Draft Recommended Practice for
Electronic Power Subsystems:
Parameters, Interfaces, Elements, and Performance

1. Overview

1.1. Scope
This recommended practice provides a technical basis for implementation of electronic power subsystems. It is intended for electronic systems engineers and integrators, electronic power subsystem designers and integrators, as well as power element manufacturers and suppliers. It addresses system-level issues in element or subsystem integration, adaptation, and accommodation. It also defines system interface parameters, test methods, and test conditions.

This recommended practice applies to ac-dc and dc-dc electronic power subsystems. The range of electronic power subsystems includes those with dc, single-phase, and three-phase inputs, with having power levels from a fraction of a watt up to 20 kW. The voltage range is 600 V and below, at a frequency or frequencies of dc - 1 kHz. Internal operating frequencies within elements or subsystems may be much higher than 1 kHz.

This recommended practice may be used outside the range where applicable.


1.2. Purpose
The purpose of this recommended practice is threefold: (a) to provide a systems engineering approach to acquisition, adaptation, and integration of electronic power subsystems, (b) to facilitate and promote a modular approach to element or subsystem integration, and (c) to enable effective communication between the end users of power electronics and their manufacturers or suppliers.

1.3. Organization of this recommended practice
This recommended practice is organized into ten clauses and five annexes.
Clause 1 is an overview of the scope, purpose, and organization of this recommended practice.
Clause 2 lists the references that should be consulted when using this recommended practice.
Clause 3 identifies acronyms and terms used throughout the text of this recommended practice.
Clause 4 contains parameters that are at element level. These parameters can be added to IEEE Std. 1515-2000 upon its revision.
Clause 5 identifies essential considerations for designing and implementing electronic power subsystems in the areas of requirements definition, architectural considerations, and system interaction. Four interfaces are defined: electrical interface, mechanical interface, environmental interface, and system effectiveness interface.
Clause 6 identifies electrical interface parameters related to electrical interactions between elements, or between an element and its higher level subsystem, including parameter definitions, test methods, and test conditions.
Clause 7 presents mechanical interface parameters related to mechanical interactions between elements, or between an element and its higher level subsystem.
Clause 8 presents environmental interface parameters that concern the subsystems’ local conditions such as temperature, humidity, vibration, and dust.
Clause 9 contains system effectiveness interface parameters including reliability, logistics, and methods to predict or extend the life cycle of a subsystem.
Clause 10 discusses system integration issues of electronic power systems design and specification. It is intended to cover the major issues of concern and provide guidance to the designer as to the applicability of commercial items.
Clause 11 discusses adaptations that can be made to any or all of the system interfaces described in Subclause 5.1. The benefits of adapting a commercial item must be favorable with regard to a custom development considering schedule, risk, performance, and total cost.

Annex A is a list of additional readings (bibliography) that one may find helpful in understanding this recommended practice.

Annex B provides a list of performance parameters. It provides performance levels that are “commonly available” (from manufacturer’s catalog items). This allows designers to use this recommended practice to determine the extent that an existing product (element) may be used to configure a particular electronic power subsystem. The data are dynamic and they change with technology.

Annex C is an index for all the parameters that are defined in both IEEE Std. 1515-2000 and in P1573.

Annex D is a brief summary of definitions, test methods, and commonly used corrective actions related to (nuclear) radiation effects for natural as well as man made radiation effects on electronics.
2. References

This recommended practice should be used in conjunction with the following publications. If the following publications are superseded by an approved revision, the revision shall apply.

Although current practice favors the use of commercial and/or international standards, several military standards are ubiquitous to the commercial market. As an example, MIL-STD-883 is widely used in both commercial and military electronics test and qualification activities.


3. Definition of abbreviations, acronyms, and terms

The terms collected here are not all inclusive of the terms used to describe an electronic power distribution subsystem. Additional terms can be found in Handbook of Standardized Terminology for Power Sources Industry published by the Power Sources Manufacturers Association (PSMA).
Abbreviations and acronyms frequently encountered are also included for easy reference.

3.1. Acronyms

A   ampere
ac   alternating current
ASIC  Application-Specific Integrated Circuit
ASSL  abnormal steady state limit
ATP   Acceptance Test Procedure/Plan
BABT  British Approvals Board for Telecommunications (Certification Company)
BIT   built-in-test
BW    Bandwidth
°C    degrees centigrade
CB    circuit breaker
CCA   Circuit Card Assembly
CE    European Union Conformity Mark (European Commission)
CFM   Cubic Feet per Minute
CG    center of gravity
CI    commercial item
CM    Common Mode
COTS  Commercial-Off-The-Shelf (equivalent to CI)
CSA   Canadian Standards Association
dc    Direct Current
di/dt  Rate of Current Change
DIN   Deutsche Institut fur Normung (German Standards Institute)
DIP   Dual In-Line Pins
DM    Differential Mode
EMC   Electromagnetic Compatibility
EMI   Electromagnetic Interference
EPSS  Electronic Power Specification Standardization
ESD   Electrostatic Discharge
ESS   Environmental Stress Screening
ESSL  emergency steady state limit
ET    Elapsed Time
FAR   Federal Acquisition Regulations
FCC   Federal Communications Commission
FIT   Failure in Time
GIDEP Government-Industry Data Exchange Program
HALT  Highly Accelerated Life Test
HASS  Highly Accelerated Stress Screening
HCP   horizontal coupling plane
3.2. Terms

3.2.1. Combined effects
Combined effects are the condition where two or more parameters are considered to be acting on the element at issue to influence performance. Power density is the ratio of total rated output power to the physical volume of the electronic power subsystem, including all interface requirements imposed by the identified electronic power subsystem. This normally includes EMI filters and heat exchanger volume. A given electronic power subsystem can have different power density ratings in different applications.

3.2.2. Commercial component
Any component that is a commercial item [2].

3.2.3. Commercial item
Any component that is a commercial item [2].

Commercial item means:
- Any item, other than real property, which is of a type customarily used for non-governmental purposes and that
  - Has been sold, leased, or licensed to the general public; or,
  - Has been offered for sale, lease, or licensed to the general public;
- Any item that evolved from an item described in paragraph (a) through advances in technology or performance and that is not yet available in the commercial marketplace, but will be available in the commercial marketplace in time to satisfy the delivery requirements…
- Any item that would satisfy a criterion expressed in paragraphs (a) or (b) of this definition, but for –
  - Modifications of a type customarily available in the commercial marketplace; or
  - Minor modifications of a type not customarily available in the commercial marketplace
3.2.4. Commercial off-the-shelf
Items which can be purchased through commercial retail or wholesale distributors, as is, and are generally available as a catalog item [3].

3.2.5. Cooling medium
Cooling medium is the material used to transfer heat in a heat flow path.

3.2.6. Electrical terminations
Physical attachments to achieve electrical interface connections.

3.2.7. Element
An element is an accessible building block of an electronic power subsystem. Depending on the context, usage or the intended use, it can be referred to as component, circuit card, assembly, subsystem, or product. The functions and features of an element can be unambiguously defined at its interfaces by the corresponding interface parameters. An element could be acquired as either a commercial or a custom item and where its features and function could be subjected to adaptation to accommodate specific demands of the intended applications.

3.2.8. Input voltage spikes
Input voltage spikes are bi-directional voltage levels of a shorter duration than transients. Spikes can be caused by lightning strikes, inductive kicks, load changes, or any other input line voltage abnormality. Spikes typically can be suppressed by unidirectional or bi-directional transient suppressors metal oxide varistors (MOV), bipolar transient absorbers, and gas discharging tubes.

3.2.9. Input voltage transients
Input voltage transients are voltage levels that are outside steady state levels. Since it is a transient, it will not be sustained for a steady state condition. These transients are generally random in nature and have a duration of up to seconds; however they typically result in very low duty cycles, less than 1%.

3.2.10. Logistics
Logistics is the discipline of planning and accomplishing acquisition, storage, movement of materials, and the maintenance of systems.

3.2.11. Platform
A platform is an end using system such as an airplane, an automobile, a battle tank, a satellite, medical equipment, etc.

3.2.12. Power density
Power density is the ratio of total rated output power to the physical volume of the electronic power subsystem, including all interface requirements imposed by the identified electronic power subsystem. This normally includes EMI filters and heat exchanger volume. A given electronic power subsystem can have different power density ratings in different applications.

3.2.13. Supportability
The degree to which system design characteristics and planned logistics resources support system operations and readiness needs throughout the system’s service life at an affordable cost.

3.2.14. Synchronization of elements
Operation of power electronic elements at a common frequency or multiple of a common frequency, achieved via a synchronization signal between elements and/or the external interface.
4. Element-level parameters

Parameters defined in this subclause are all at element level. They should logically belong to the companion document of IEEE Std 1515-2000. This can be done upon its revision.

4.1. Set point voltage accuracy

4.1.1. Definition

Set point voltage accuracy is the ratio of the measured to the nominal output voltage, \( \frac{V_m - V_n}{V_n} \times 100 \). (See also IEEE Std. 1515-2000, Subclause, 4.4.2.)

4.2. Maximum power dissipation

4.2.1. Definition

The amount of power that will be dissipated by the electronic power subsystem under the combined specified conditions. (See IEEE Std. 1515-2000, Subclause, 4.3.2.)

4.3. Contact resistance

4.3.1. Definition

The electrical resistance found between two mating surfaces.

4.3.2. Test method

Apply a current equal to the mated rating of the connecting feature (pin, screw terminal, bus bar) and measure the voltage drop across the junction of the connection using a 4-wire method. The value obtained by dividing the measured voltage drop by the current applied represents the contact resistance.

4.3.3. Test condition

Per IEEE Std. 1515-2000, Subclause 4.7.1

4.4. Input undervoltage protection

4.4.1. Definition

Undervoltage protection is the function of a component or circuit in an electronic power subsystem designed to sense and provide protection against an input voltage that is below the level of normal or safe operation. Protection is achieved by shutting down or reducing operating stress.

4.4.2. Test method

Connect the test setup as shown in Figure 1. Use a DMM that measures the dc voltage or root mean square (RMS) value of an ac voltage input to the unit under test (UUT). With the input to the UUT initially adjusted to nominal voltage, slowly decrease the input. Record the voltage level at which the UUT generates an input undervoltage signal and verify that the UUT has shutdown. Some UUTs will actually continue to operate at low input voltages until the output voltage decreases to a level that generates an output undervoltage signal. Readjust the input voltage to nominal and verify the response of the UUT. Some UUTs will reset themselves and return to normal operation, while in other UUTs the fault may latch up and wait for a restart command to recover to normal operating conditions.
### 4.4.3. Test condition
Operate and tests the UUT over the full temperature range. The load shall be adjusted from $I_{\text{min}}$ to $I_{\text{max}}$.

### 4.5. Input overvoltage protection

#### 4.5.1. Definition
Input overvoltage protection is a circuit function in an electronic power subsystem designed to sense an input voltage that is above the level of normal or safe operation and provide protection, for example by shutting down or reducing operating stress.

#### 4.5.2. Test method
For a steady state input overvoltage test use the test setup shown in Figure 2. Use a DMM that measures dc voltages, or the RMS value of an ac voltage across the UUT input. In either case of operation, slowly increase the UUT input voltage and record the voltage level at which the UUT generates an input overvoltage signal. In some UUTs the fault may latch-up and turn off the UUT. Readjust the input to nominal and verify the response of the UUT. Some UUTs will reset themselves; others wait for a restart command to recover to normal operating conditions.

Refer to IEEE Std 1515-2000, Subclauses 4.15.2.2 and 4.15.3.2 for an output overvoltage test method.
4.5.3. Test conditions

Adjust the input voltage to nominal conditions. Operate and test the UUT over the full temperature range. The load shall be adjusted from $I_{\text{min}}$ to $I_{\text{max}}$. For output overvoltage test conditions, refer to IEEE Std 1515-2000, Subclauses 4.15.2.3 and 4.15.3.3.

4.6. Overtemperature shutdown

4.6.1. Definition

An overtemperature shutdown is a feature of protection that causes the subsystem to automatically shut itself down if the temperature at a defined monitoring point exceeds a pre-determined temperature threshold. At recovery, there is usually hysteresis. This fault condition is usually reported to a monitoring system by the subsystem as a failure. An overtemperature shutdown is a function that causes the power system to automatically shut itself down if the temperature at a pre-determined monitoring point exceeds a pre-set threshold.

4.6.2. Test method

Use a temperature chamber to perform the tests. Connect the test setup as shown in Figure 3. With the DMM or oscilloscope measure the output voltage. Attach the thermocouples directly to the defined location of interest on the UUT to measure and use the thermometer to record the temperature at which the UUT shuts down. To conduct the test, slowly increase the ambient temperature in the chamber while operating the UUT under the desired test conditions. Some UUTs may generate an overtemperature signal and shut off when the fault occurs. Others may only shut off at the temperature limit of operation. Cooling the UUT, verify and record the temperature at which the UUT restarts itself. In some UUTs the fault may latch-up and only turn back on with a restart command.

Monitor the temperature rise of the base-plate to protect the UUT by turning off the power source in case the UUT thermal protection mechanism malfunctions.
4.6.3. Test condition
Per MIL-STD-810E (Method 520).

4.7. Reverse voltage protection

4.7.1. Definition
Reverse voltage protection is a function performed by a circuit or circuit component to protect the electronic power subsystem from any damage that can be caused by the application of a voltage of reverse polarity at the subsystem’s input or output terminals.

Two examples of input reverse polarity protection are a shunt diode or a diode in series with the input of the UUT. An example of output reverse polarity protection is the addition of a rectifier outside the output filter of the UUT.

4.7.2. Test method (input reverse voltage)
For input reverse voltage protection, connect the test setup as shown in Figure 4. Use a current-limited source or add a fuse or circuit breaker with the appropriate voltage/current rating in series with the input of the UUT. Begin by adjusting the power source output voltage to zero. Turn on the UUT. Swap the output leads from the power source as shown in Figure 5. Verify that as the power source output voltage is slowly increased the UUT withstands the reverse polarity condition without failure. Repeat the test, adjusting the power source voltage to the steady state range prior to application to the UUT. A programmable voltage source or suitable switching device should be used.
4.7.3. Test method (output reverse voltage)

For output reverse voltage protection, connect the setup as shown in Figure 6, with a test power supply connected in reverse polarity to the output of the UUT. If necessary, apply a minimum load to the UUT. Turn on the power source and UUT, and verify the UUT operates normally with a nominal input voltage. Turn on the test supply and slowly increase the output of the test supply up to the maximum reverse voltage rating of the UUT while monitoring the current drawn from the test supply. Confirm the current drawn from the test supply is as expected – a high current if the UUT is protected by a shunt element across its output, but a low or zero current if the protection is by a series blocking element (diode, MOSFET or similar). If the UUT has a reverse voltage indicator verify it turns on at the expected voltage level. Reduce the voltage of the test supply to zero and confirm that the UUT returns to normal operation.
4.7.4. **Test condition (input reverse voltage)**
For input reverse voltage protection, adjust the load current to $I_{\text{min}}$.

4.7.5. **Test condition (output reverse voltage)**
For output reverse voltage protection, adjust the input voltage to the UUT to nominal. Adjust the output load to minimum.

4.8. **Turn-on time**
Turn-on time is the time it takes to begin operating within the specifications after the proper power has been applied.

4.9. **Regulation, combined**

4.9.1. **Definition**
The sum of the effects of line, load, and temperature regulation as defined in IEEE Std. 1515-2000, Subclauses 4.4.1 through 4.4.3 respectively.

4.9.2. **Test method**
Per IEEE Std. 1515-2000, Subclauses 4.4.1 through 4.4.3.

4.9.3. **Test condition**
Per IEEE Std. 1515-2000, Subclauses 4.4.1 through 4.4.3.

4.10. **Regulation effects due to aging**

4.10.1. **Definition**
Regulation effects due to aging are degradation in combined regulation due to life or long term effects.

4.11. **Lightning**

4.11.1. **Definition**
Lightning is a natural phenomenon that occurs when electrical potential energy is discharged directly to the ground or through another object. A lightning strike is a large current that increases voltage potential between two points in a subsystem due to high-level current flow. The series impedance is the dominant factor for voltage spikes since lightning strikes may range as high as 100kA. (The largest spike recorded was 3MA, but this is a rare occurrence.)
4.12. Surge

4.12.1. Definition
A surge is a sudden voltage increase on the power mains. A surge is limited by the source impedance and has the greatest affect on the loads with the lowest input impedance. They are often caused by load changes that are a small percentage of the total load capacity.

4.13. Sag

4.13.1. Definition
Sag is a sudden decrease in input voltage due to increased load on the main power subsystem. Long lasting sags may be referred to as brown-out.

4.14. Transients (spikes)

4.14.1. Definition
Transients are short duration surges or sags of input voltage during the period of changing load conditions in an electrical or electronic system or from other sources. Turning on equipment that has large in-rush current causes a negative voltage step on the mains usually called a transient. The turn-off or shedding of inductive loads causes a positive voltage step. The magnitude of the voltage step transient is derived from the impedance of the source and the magnitude of the current non-repetitive deviation from steady state.
5. Electronic power subsystems

Electronic power subsystems are an integral part of electronic systems. All electronic systems, whether medical, telecom, automotive, avionics, or consumer electronics, or whether military, industrial, or commercial, require electrical power to operate.

An electronic power subsystem is a collection of power elements that convert, manage, and distribute electrical power from the input source to load.

This clause identifies essential considerations in designing and implementing electronic power subsystems. It focuses on the interface issues among elements of an electronic power subsystem and between a subsystem and its user-level electronic system.

It is beyond the scope of this recommended practice to discuss the internal aspects of elements that compose an electronic power subsystem or to specify their design. However, there are methods to facilitate matching existing elements to application requirements. These methods fall into the categories of requirements definition, architecture selection, and consideration of system interaction and logistics. These methods are discussed as they pertain to the interfaces between a user-level electronic system and an electronic power subsystem, and to the interfaces between elements within a subsystem.

Since one of the purposes of this recommended practice is to facilitate implementation of electronic power subsystems using commercial items in demanding applications, this clause and several of the follow-on clauses, specifically Clause 11 contain adaptation approaches to allow use of such elements in applications beyond that for which they were intended. The use of commercial items can reduce technical and schedule risk, as well as total cost.

Subclause 5.1 defines the four interfaces, in simple terms, which apply to subsystems and elements. Subclause 5.2 discusses an important issue in electronic power subsystem development, requirements definition. Subclause 5.3 discusses architectural considerations for a successful development of an electronic power subsystem. Subclause 5.4 provides top-level details on the important issue of system interaction.

5.1. Interface definition

Interface refers to connections and interactions between elements, or connections and interactions between elements and the higher-level subsystem.

In this recommended practice, interfaces are organized into four categories. They are the electrical, mechanical, environmental, and system effectiveness interfaces. In order for an element to function as expected, the four interfaces need to be adequately defined, the requirements imposed on the interfaces need to be satisfied, and both normal and fault conditions need to be addressed.

It is noted that the electrical interface and mechanical interface are physical interfaces in the sense that they are integral to the element. The environmental interface is physical but not all aspects of the environmental interface may be present in a given utilization scenario. The system effectiveness interface is a virtual interface that is descriptive of performance metrics such as efficiency, failure rates, mean-time between failures, mean-time to repair, etc.

Figure 7 is a simplified diagram that illustrates the relationship between these interfaces and an element.

It should be noted that interfaces are bi-directional. In other words, a higher-level subsystem can affect the operation of an element and vice versa.

In practice, by specifying interface parameter performance and variations, it can be determined whether a particular element can meet the requirement with or without adaptation. Table 1 lists examples of issues and parameters that should be considered in the development and integration of electronic power subsystems.
Figure 7. Relationship between an element and its interfaces

Table 1. Example interface considerations

<table>
<thead>
<tr>
<th>Electrical</th>
<th>Mechanical</th>
<th>Environmental</th>
<th>System Effectiveness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage range</td>
<td>Dimensions</td>
<td>Operating temperature range</td>
<td>Reliability</td>
</tr>
<tr>
<td>Input frequency range</td>
<td>Thermal interface</td>
<td>Storage temperature</td>
<td>Life expectancy</td>
</tr>
<tr>
<td>EMI/EMC</td>
<td>Structural requirements</td>
<td>Humidity</td>
<td>Regulatory requirements</td>
</tr>
<tr>
<td>Input voltage/ frequency transients</td>
<td>Mounting</td>
<td>Shock</td>
<td>Component quality</td>
</tr>
<tr>
<td>Output voltage and current</td>
<td>Power dissipation</td>
<td>Vibration</td>
<td>Configuration management</td>
</tr>
<tr>
<td>Efficiency</td>
<td>Center of gravity</td>
<td>Salt spray</td>
<td>Derating</td>
</tr>
<tr>
<td>Control and status signals</td>
<td>Cooling medium</td>
<td>Explosive atmosphere</td>
<td>Component/Product Obsolescence</td>
</tr>
<tr>
<td>Dynamic load and signal requirements</td>
<td>Weight</td>
<td>Radiation</td>
<td>Quality assurance</td>
</tr>
<tr>
<td>Overcurrent/ overvoltage protection</td>
<td></td>
<td>Sand and dust</td>
<td>Safety</td>
</tr>
</tbody>
</table>

5.1.1. Electrical interface
The electrical interface includes connections and interactions between elements, or between an element and its higher level subsystem, that can be described by electrical parameters, such as voltage, current, and power. The electrical interface may also include control signals that will change the electrical operating conditions of the element and higher level subsystem. It may also include the means to measure and change the operation of an element to ensure its proper operation, such as test points in the manufacturing process.

The electrical interface between elements, or between an element and its higher level subsystem, can be illustrated as shown in Figure 8.
For any given electronic power element, the input and output are typically voltage and current. There may also be control signals from the system to change the operating conditions of an element and or signal(s) from an element to the system to indicate its status.

Note that bi-directional arrows are used for $V_{in}$, $I_{in}$ and $V_{o}$, $I_{o}$ to indicate that there will be electrical interaction between an element and the system. An example is a power supply that converts one voltage level to another level to power digital circuits. In this case, the power supply takes the voltage and current from the system (the influence from the system) and provides another voltage level to power the digital circuits (the function of the element). The power supply will generate EMI noise affecting the system and it will also change the impedance of the system bus affecting both voltages and currents at every node in the system; these are influences from a particular element.

5.1.2. Mechanical interface

The mechanical interface is defined as connections and interactions between elements, or between an element and its higher level subsystem, that can be described by mechanical parameters, such as size, mounting methods, thermal aspects, and internal and external connections.

Note that there may be significant interaction between any given element and the system. This is a particularly important consideration at the system definition and initial system design stage.

Human-Machine Interface (HMI) requirements should also be considered. One HMI requirement of the mechanical interface could be the ease of installation, and removal.

5.1.3. Environmental interface

The environmental interface encompasses the interactions between an element and its higher level system that can be described by environmental parameters, such as temperature, altitude, and humidity. Operating and non-operating environments are among the environmental parameters to be defined. There may be several different environments within one platform such as manned vs. unmanned areas of vehicles. Environmental conditions influence life expectancy, robustness and reliability.

5.1.4. System effectiveness interface

The system effectiveness interface includes logistics, support, and life cycle parameters driven by design trade-offs and interactions among the three other interfaces that contribute to the functionality of an electronic power subsystem for a given application.

System effectiveness interface is a broad concept. It covers the issues that are not covered in the three other interfaces. The system effectiveness interface can be divided into two areas. One includes system-level issues that are not directly related to the above three interfaces, such as product life, warranty, system configuration management, cost, schedule, etc. The other includes connections and interactions among the above three interfaces in order to achieve best system-level performance.

Some of the examples of system effectiveness interface are:
- The logistics of the program, technical support and lifecycle maintenance of the product
- The schedule of the program and the element and system configuration management
- System design aspects such as the inclusion of built-in-test, and the system software capability
- System quality and derating
- Impact of failure – failure modes, effects and criticality, system redundancy, etc.

Some other more detailed examples of the system effectiveness interface include the following:
Advanced pins are often used in the system to allow certain circuits of the element to contact the system first during plug-in. One such example is the advanced pins for power connection. Similarly, in some cases, retarded pins are used to achieve the opposite objective.

Mechanical interlock is sometimes used to ensure that the electrical operations of the element can be achieved only after the element is seated properly into the system. In some other cases, interlock is used in the system so that the element cannot be removed from the system before it terminates electrical functionality.

Overtemperature shutdown of the power element is an example of the inter-reaction between the electrical interface and the environmental interface. In this case, the environmental parameter (temperature) influences the operation of the electrical function of the element.

It should be emphasized that system effectiveness interface parameters can be complicated and are sometimes mutually conflicting. A systematic approach is usually required and strongly recommended to define and achieve an optimal system effectiveness interface.

5.2. Requirements definition

Requirements definition is the process of identifying application, interface, and regulatory requirements and constraints. Defining requirements clearly is a primary task for successful completion of subsystem development. The requirements definition generally results in a specification for the electronic power subsystem.

The requirements definition process begins at the interface between the electronic power sub-system and the related system. All parameters of this interface should be considered including electrical input and output; mechanical aspects; environmental exposure; and system effectiveness. Where applicable, normal operating extremes and worst-case transient limits should be identified. Requirements should subsequently be defined for each of the elements of an electronic power subsystem, as appropriate. These requirements are derived from requirements at the subsystem interface and from constraints imposed by the architectural design. Analysis and/or prototype system-level tests may be required to derive the requirements of the individual element(s) from the total subsystem requirements.

Guidelines for successful requirements definition include specifying interface parameters as openly as practical while adequately specifying, and involving manufacturers of building block elements under consideration in trade-off decisions during the requirements definition process. Requirement definition and the power subsystem product concept should be worked in parallel so that limitations imposed on the concept by requirement, can be fully understood and challenged before either the requirements or the concept is frozen. An iterative process of requirements definition and subsystem architecture is critical to increasing the probability of successful use of commercial item elements. This process generally involves the participation of the subsystem designer, the customer, application end-user, and element providers jointly participating in requirements definition and trade-off studies.

Overspecification is potentially a limiting factor at each level in the development process, particularly when considering the use of commercial items (CI). The requirements definition process should anticipate system evolution and accommodate potential changes with minimal design impact. Proper requirements definition covers all parameters of all the interfaces of a subsystem. A parameter that is not defined may take values outside the acceptable ranges for well behavior of systems. It may cause unpredictable behavior of the subsystem and may ultimately result in catastrophe.

Overspecification is mitigated by providing common terminology and definitions for subsystem parameters and by identifying parameters requiring quantification. Typical parameter values commonly available in commercial items are included in Annex B. Caution, however, is urged in the use of these “typical” parameter values. They represent the commercial market at a particular element level at the time of issuing this recommended practice. Further, subsystems defined by combinations of these parameter values may be neither commercially available nor economically achievable. For example, typical values for power density or reliability available in low level building block elements will generally have to be re-evaluated for subsystems built with combinations of these and other elements. The observed common trend is for subsystem reliability and efficiency, relative to single constituent element, to decrease as elements are combined to form subsystems. Unless proper attention is paid to the thorough definition of requirements, it is likely that the performance, reliability and efficiency of the power subsystem will be compromised, and the final cost will be unnecessarily high.
5.3. Architectural considerations

An electronic power subsystem architecture is driven by the defined requirements and architectural strategies, including planned technology insertion. Often the architectural choices open to the designer are constrained by non-technical system requirements or constraints such as prior decisions, system architecture and packaging, or schedule. Even when the constraints are limited to the technical aspects of an electronic system interface, more than one architectural approach will usually meet the interface requirements. Choosing among these architectures is primarily an optimization process, usually involving parameters that are difficult to quantify accurately during conceptual design in areas such as life cycle cost, reliability, and obsolescence. The life cycle goals of the application and associated system, and customer decision criteria should be understood when performing the trade-off analysis.

An electronic power subsystem architecture is the methodology by which the input power source is converted to load power requirements, within the constraints imposed by the four subsystem interfaces. Architectural choices range from highly integrated to modular solutions. Highly integrated architectures may achieve the best performance and lowest recurring unit cost but may not be adaptable to evolving electronic system requirements. When such evolution or technology insertion is anticipated at the electronic system-level, a modular solution involving multiple physical elements may be preferable, even if achieved at higher initial acquisition cost.

The approach diagrammed in Figure 9 is a block schematic example of a highly integrated solution for a four-output ac to dc converter requirement. The simplified schematic example illustrates a power conversion scheme involving a single conversion stage with isolation, regulation, and filtering accomplished using a single integrated magnetic device. The success of such an approach relies on optimization of the magnetic and circuit design to the application specific load voltages and currents, including knowledge of minimum loads and cross loading extremes. The specificity of such an approach to the application requirements usually requires a custom development with its associated cost, risk, and schedule. Subsequent changes due, for example, to system evolution will generally require significant product redesign.

![Figure 9. Highly integrated power subsystem](image)

The approach diagramed in Figure 10 accomplishes the same power conversion requirement with a modular architecture. In this example, a non-isolated boost converter performs conversion of the input ac voltage to an intermediate dc link voltage. The dc link is followed by independent isolated dc-to-dc converters for three of the four outputs with the forth output provided by a non-isolated dc-to-dc converter sourced by output number two.
This approach involves multiple stages of conversion and duplication of circuit functions when compared to that of Figure 9. Such duplication will generally result in higher recurring product cost, however, total cost may be lower when the initial development cost and evolutionary requirement changes are considered. The lower development and redesign costs assume that the modular building blocks are either commercially available or exist in a standard circuit design library. Even the recurring product cost may be lower when the individual building block modules are available commercially from high volume manufacturing lines.

Figure 10. Modular power subsystem

These two examples represent divergent approaches with regard to the architectural choice of integrated versus modular architecture, yet each approach is valid. The integrated approach, for example, is appropriate for high volume cost sensitive applications, especially “disposable” products or those with limited product life. They may also be appropriate when the application requirements cannot be met by available modules or when available modules cannot be adapted to particularly demanding aspects of an application's requirements, such as environmental extremes. Architectural choices can facilitate the use of commercially available items.

A major architectural option is the choice between centralized versus distributed electronic power subsystems. Centralized solutions combine all stages of conversion in a common element, usually a circuit card or enclosure including one or more circuit card assemblies (CCA). Distributed solutions are characterized by use of a final conversion stage onboard the electronic system circuit cards. Distributed architectures may convert the input source to an intermediate voltage or the input source may be distributed directly to the electronic system circuit cards for onboard voltage conversion. Highly integrated architectures are necessarily centralized. Modular architectures may be either centralized or distributed. The majority of electronic power subsystems are a hybrid of centralized and distributed approaches. In a hybrid architecture, an electronic power subsystem element converts the input source to one or more outputs for use throughout the electronic system, while other system load voltages are locally derived.
either from the input source, another system load voltage, or an intermediate voltage. Figure 11, Figure 12, and Figure 13 shows examples of centralized, distributed, and hybrid architectures.
Figure 11. A typical centralized architecture for electronic power subsystems

Figure 12. A typical distributed architecture for electronic power subsystems
Centralized architectures most often require custom solutions, though it is often possible to construct the custom solution using commercial item power electronic elements as building blocks. Centralized solutions may facilitate standardized approaches at the electronic system-level. Open system architecture approaches, such as VME, specify a standard compliment of dc voltages (+5, +/-12, +3.3) and standard system interface and BIT signals that favor a centralized electronic power subsystem approach. Centralized architectures often result in the lowest recurring hardware cost for the electronic power subsystem, though it may not result in the lowest life cycle cost. Centralized solutions typically have higher development costs and longer development time, and are less adaptable to change. Such architectures may accommodate changes by use of replaceable modules or programmable outputs.

Distributed solutions facilitate the use of commercial items, particularly at latter stages of conversion. The distributed voltage is generally limited by safety or other requirements thus requiring an initial conversion stage(s) when the input source voltage is other than the distributed voltage. Distributed architectures are ideal for systems requiring battery back up. The distribution voltage in such a system is typically the battery charge voltage. Additional benefits of distributed approaches include distribution of the heat load, easier implementation of redundancy, easier regulatory compliance (through use of pre-approved elements), and lower development cost but with potentially higher recurring costs. Distributed electronic power subsystem architectures may dictate a custom solution at the electronic system-level due to the requirement for a common distributed bus voltage, and embedding final stages of the electronic power subsystem within the electronic system.

Many electronic power subsystems are a hybrid of distributed and centralized approaches. A first stage of conversion may be used both to generate a distributed voltage bus and to supply a number of lower power and/or higher voltage buses. The distributed voltage bus can then be used to supply dc-to-dc converters located near the point of use within the electronic system for low voltage, high current loads. This type of system is used in some personal computer supplies, where a centralized power element converts the ac source to dc voltages, for the
display, and provides an isolated intermediate dc voltage bus for distribution to dc-to-dc converters, located near the low voltage, high current processing loads.

The pace of technological change and component obsolescence dictate that modern systems with long intended lifespans must be designed with planned technology insertion in mind. This often means accommodating lower dc voltages in future iterations. As system voltages continue to fall and current demand increases, centralized solutions will become increasingly difficult to implement. In such cases, distributed dc-to-dc converters at the point of use may be required for the final generation of the low voltage.

Attention to architectural decisions are essential to successful electronic power subsystem implementation, particularly when considering the use of commercial item elements. Element interfaces, as defined in this recommended practice, are electrical, mechanical, environmental, and system effectiveness. Interface performance may not ideally map from an application’s requirement to an element’s capability. Mapping between these interface requirements and available performance may be possible with specific architectural arrangements of available elements and by providing additional circuitry, or other adaptations, between system and element interfaces.

Figure 14 depicts these interfaces and represents adaptations. Examples of methods for mapping required interfaces to available elements are provided in Table 2 and discussed in further detail in Clause 11.

An example that includes electrical adaptations to allow use of widely available telecommunications dc-to-dc converter elements in applications that traditionally do not use them is provided in Figure 15. Such an approach could be implemented in either centralized or distributed system architecture.

Figure 14. Electronic power element interfaces and system adaptation

Table 2. Architectural interface adaptations

<table>
<thead>
<tr>
<th>Interface</th>
<th>Example Adaptations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td>Transient protection, filtering, voltage translation (up/down conversion), galvanic isolation</td>
</tr>
<tr>
<td>Mechanical</td>
<td>Vibration damping, heatsinking, encapsulation</td>
</tr>
<tr>
<td>System Effectiveness</td>
<td>Redundancy, derating, built-in-test (BIT), programmability</td>
</tr>
<tr>
<td>Environmental</td>
<td>Special cooling, moisture control, shock reduction; conformal coating, encapsulation, vibration damping, bonding</td>
</tr>
</tbody>
</table>
5.4. System interaction

Combining electronic power subsystem elements that operate as specified in isolation may create significant problems due to adverse interactions between the elements. Potentially adverse system interactions can occur in each of the four defined interfaces.

Electrical interactions may result in subsystem instability, load imbalance for parallel converters, noise coupling, and electromagnetic interference. Subsystem instability can occur particularly in distributed architectures when the negative impedance of a converter loads is incompatible with the converter’s source impedance and or distributed impedance. (This concern is further addressed in Subclause 10.1.)

Where elements (usually dc-to-dc converters) are used in parallel to either increase output current or to provide redundancy, load imbalances are possible in either normal-operating modes or fault modes. Such imbalance can result in unacceptable thermal conditions, high ripple, and/or voltage oscillations. Load sharing methods are often used to mitigate this concern and are addressed in Subclause 10.1.2.

The high frequency switching converter elements, frequently used in electronic power subsystems, are sources of electrical noise from which the system usually requires protection. The same concern exists within the subsystem where elements, particularly control and monitoring circuitry, require protection from other elements. Filtering, shielding, and synchronization (for fixed frequency converters) are among the methods used to mitigate these issues.

Mechanical interactions may include effects such as thermal and structural coupling, material incompatibility (e.g., dissimilar metals), and mismatch of thermal coefficients of expansion. Whenever multiple elements are integrated into a common physical assembly the thermal and structural environment is elevated above that of the interface to the assembly of the subsystem or system. The thermal and structural interface for an individual element is dependent on the physical structure of the assembly and on influences of the other elements. Therefore, analysis and or test of the integrated system should be performed. When indicated, packaging methods to mitigate these effects can be incorporated including cooling, vibration isolation, or stiffening of the assembly and are addressed in Subclause 11.2.

Environmental effects are usually viewed as phenomena imposed on a subsystem. There are, however, undesirable responses to the imposed environments due to certain combinations of elements. Such responses include outgassing and nutrient growth due to organic materials. An example is the potential for explosive conditions when a non-hermetic relay is used in conjunction with an element that can create hydrogen outgassing, such as an aluminum electrolytic capacitor in fault mode.
System effectiveness concerns may include life cycle issues such as cost, reliability, maintainability, and testability. These issues are driven by the system effectiveness capability of individual elements, by the combination of the elements, and by the method of interconnection. Parallel connections of elements can adversely affect testability due to the inability to determine which element has failed. System effectiveness issues and methods that mitigate one issue may compromise another. Reliability, for example, can be enhanced beyond that of individual elements through redundant configurations, although cost and testability may be impacted. Complete system-level analysis and appropriate tests are required to prove system functionality and integrity according to applicable specification at all levels of system integration.
6. Electrical interface parameters

Electrical interface parameters related to electrical interactions between elements, or between an element and its higher level subsystem, are described herein. Where illustrative, test methods and test conditions are described. Electrical interface parameters usually considered at the element level are defined in IEEE Std. 1515-2000. Annex C, Table C-1, Table C 2, and Table C-3 of this document are directories to the locations of electrical interface parameters described in either this recommended practice or IEEE Std. 1515–2000.

6.1. Status monitoring

Status monitoring is the capability to detect that essential parameters of the electronic power subsystem are within pre-determined limits, and provide an indication if one or more of the monitored parameters is outside the pre-determined limits. This capability may also provide an indication if a failure is detected in a subsystem or an element, even if performance parameters remain within the predetermined limits.

6.2. Supervisory control

Supervisory control is the capability to allow alteration of one or more parameters of the electronic power subsystem to meet system-level performance objectives. This may be achieved through a local or a remote control interface. Examples include remote resetting of protection circuits, remote on-off capability, alteration of output voltage and or current settings, etc.

6.3. Built-in-test

6.3.1. Definition

Built-in-test (BIT) is the capability to exercise all or part of a system (in this case, an electronic power subsystem) in order to determine whether it is functioning correctly. It is implemented by providing additional dedicated circuitry or software, separate from that required, to achieve the normal functionality. BIT capability may be intended for use only during production testing, or it may be intended to run periodically or on demand, as part of routine maintenance. Examples include exercising of redundant or standby elements, checking of battery capacity, testing of alarm circuits, etc.

The scope and complexity of BIT varies widely depending on system needs and element capabilities. Consequently it is not possible to recommend a generic test method suitable for all BIT implementation. Test methods, test condition and expected response must be defined by the designer or manufacturer. Running BIT outside the parameters specified may cause system malfunction or damage.

6.4. Electromagnetic compatibility/electromagnetic interference

Electromagnetic Compatibility (EMC) is the satisfactory operation of an element in its intended electromagnetic environment.

Electromagnetic Interference (EMI) is described as the conducted or radiated electromagnetic emissions from an element that interferes with the normal operation of another element.

Conducted emissions and susceptibility are often tested at the element level and are covered in IEEE Std. 1515-2000. Radiated emissions and susceptibility are usually tested at the system-level and are covered herein. Many sources of information are available about EMI testing and requirements. This subclause should be used as an introduction to the general topic of EMI, with the testing information serving as benchmark testing guidance prior to formal EMI testing.

The notion that EMC is mechanical is sometimes considered since shields are used for reduction or containment of radiated fields. This is somewhat misleading because, although it is often convenient to make the shield part of the supporting structure, the requirement for the shield is strictly electrical. The interest is in the shielding effect on the incident electric and magnetic waves.

Power subsystem elements such as rectifiers or switching power supplies have non-linear characteristics, and they present a complex impedance that usually changes with load. In addition, they may draw complex harmonic
currents when fed from an ac source. Their EMI performance will therefore vary as input voltage or load changes, and such variations must be considered during design and testing.

### 6.4.1. Conducted interference

Conducted interference consists of differential mode, common mode, and conducted susceptibility described herein.

#### 6.4.1.1. Differential mode interference

Differential mode interference is an undesired signal, voltage, or current passed in opposite directions, that is, out of phase, through two wires. The differential voltage is measured across the two wires; the differential current is measured in only one wire.

#### 6.4.1.2. Common mode interference

Common mode interference is an undesired signal, voltage, or current passed in the same direction, that is, in phase, through all wires. Common mode currents are measured in all wires simultaneously.

#### 6.4.1.3. Conducted susceptibility

The conducted susceptibility level of an element, at a given frequency and for a given conductor, is the level of conducted signal required to cause a system malfunction or an out of tolerance condition.

### 6.4.2. Radiated interference

Radiated interference has two aspects, emissions and susceptibility. Emissions are fields radiating from the UUT to the environment and susceptibility is the level of external fields the UUT can tolerate and still perform the desired function.

#### 6.4.2.1. Radiated emissions

#### 6.4.2.1.1. Definition

Emission of electromagnetic energy by radiation directly from the UUT, or from wiring connected to it.

#### 6.4.2.1.2. Test method

Radiated emissions tests are performed in a shielded enclosure to keep external noise sources from interfering with measuring the unit under test (UUT). MIL-STD-462D [B22] is a military that specifies for well-established methods for EMI/EMC testing. FCC Regulation 15 [B12] is a widely used method and for the European market; CISPR 22 [B13] is the governing standard for EMI/EMC testing. Antennas used for EMI/EMC testing are designed for specific test purposes such as:
- Loop magnetic fields 10 kHz to 30 MHz
- Rod or monopole 10 kHz to 30 MHz
- Bi-conical and Di-pole 20 MHz to 200 MHz
- Log-Conical or Spiral 200 MHz to 1000 MHz

#### 6.4.2.1.3. Test conditions

In a shielded room with properly grounded equipment, and with connecting cables routed away from the UUT to avoid unintentional coupling, position the antenna as shown in Figure 16, [B11], [B1], and [B13]. Type of Antenna, RF Power, and Distance between the Antenna and UUT are as specified for the particular EMI/EMC test specifications. Tests have to be conducted with UUT Power OFF to measure test pre-conditions also referred to as ambient radiation before the test is conducted with UUT Power ON. Some tests will also differentiate between a device “idle” and a device “active” state.
6.4.2.2. Radiated susceptibility

6.4.2.2.1. Definition
The radiated susceptibility level of an element, for a given source type and frequency, is the level of radiated signal required to cause a system malfunction or an out of tolerance condition.

6.4.2.2.2. Test method
Verify that the UUT can withstand the radiated magnetic and electric fields. See Radiated emissions above. Susceptibility is not considered in the FCC regulations; but is fully addressed in MIL-STD-462D.

6.4.2.2.3. Test condition
Per applicable test standard [B22].

6.4.3. Electrical noise
Any undesired electrical signal present in a circuit. These signals are not the product of non-linearity that causes distortion. Noise is produced by:
− Random fluctuations within the system (intrinsic)
− Machinery such as motors, arc welders, fluorescent lights, radio transmitters and their local oscillators
− Natural disturbances including lightning, galactic noise and ESD (Electrostatic Discharge)

6.4.4. Electrical noise spectrum

6.4.4.1. Definition
Noise spectrum is the noise amplitude vs. frequency. The spectrum to be considered in a particular application will depend upon the sensitivity of the subsystem.

6.4.4.2. Test method
A baseline measurement is taken to determine the ambient noise of a test set-up to determine if the environment is satisfactory for the measurement intended. Following ambient measurement, other measurements are taken to measure noise emissions and its effects on the affected frequency range(s). Spectrum analyzers are a class of instruments useful in measuring noise levels and frequencies.

6.4.5. Electrostatic discharge

6.4.5.1. Definition
Electrostatic Discharge is the spontaneous occurrence of current flow where a difference in dc voltage is equalized by a flow of charge between two electrically isolated bodies. This equalization is characterized by rapid current flow and may involve a spark discharge. After ESD, the voltage on the bodies is essentially equal; the primarily capacitive charge between the involved bodies having been discharged. ESD control is the process of minimizing the possibility of the occurrence of a rapid charge transfer.

6.4.5.2. Test method
Varying voltage levels are generally stored in a fixed capacitance and then applied through fixed impedance to the UUT. All externally accessible electrical interfaces to the module should be tested in accordance with the intended environment. MIL-STD-1686 [B8] as well as other industry standards were developed to specify levels of ESD and the precautions required to protect electric circuits from ESD damage. Table 3 lists ESD test standards/methods.

Table 3. ESD test standards/methods for classification of ESDS parts.

<table>
<thead>
<tr>
<th>ESD Model</th>
<th>ESD Test Standard/Method</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human Body Model (HBM), ESD CLASS 1, 2, and 3</td>
<td>EOS/ESD-S5.1</td>
</tr>
<tr>
<td></td>
<td>MIL-STD-883 Method 3015</td>
</tr>
<tr>
<td></td>
<td>MIL-STD-750 Method 1020</td>
</tr>
<tr>
<td>Machine Model (MM), ESD-S5.2</td>
<td></td>
</tr>
<tr>
<td>Charged Device Model (CDM), ESD-S5.3</td>
<td></td>
</tr>
</tbody>
</table>

6.4.5.3. Test conditions
Full characterization of the ESD susceptibility of a part is accomplished by classification to three defined models: the Human Body Model (HBM), Machine Model (MM), and Charged Device Model (CDM); see MIL-STD-1686. The HBM, MM, and CDM sensitivity classification of parts shall be in accordance with Table 4 and Table 5. The HBM, MM, and CDM voltage levels do not correlate with each other.
Table 4. ESD classification

<table>
<thead>
<tr>
<th>ESD Model</th>
<th>ESD Class (Voltage Range)</th>
</tr>
</thead>
<tbody>
<tr>
<td>HBM</td>
<td>1 (&gt;0V – 1,999V)</td>
</tr>
<tr>
<td></td>
<td>2 (2,000V – 3,999V)</td>
</tr>
<tr>
<td></td>
<td>3 (4,000V – 15,999V)</td>
</tr>
<tr>
<td>MM</td>
<td>M1 (0V – 100V)</td>
</tr>
<tr>
<td></td>
<td>M2 (101V – 200V)</td>
</tr>
<tr>
<td></td>
<td>M3 (201V – 400V)</td>
</tr>
<tr>
<td></td>
<td>M4 (401V – 800V)</td>
</tr>
<tr>
<td></td>
<td>M5 (&gt;800V)</td>
</tr>
<tr>
<td>CDM</td>
<td>C1 (0V – 124V)</td>
</tr>
<tr>
<td></td>
<td>C2 (125V – 249V)</td>
</tr>
<tr>
<td></td>
<td>C3 (250V – 499V)</td>
</tr>
<tr>
<td></td>
<td>C4 (500V – 999V)</td>
</tr>
<tr>
<td></td>
<td>C5 (1,000V – 1,499V)</td>
</tr>
<tr>
<td></td>
<td>C6 (1,500V – 2,999V)</td>
</tr>
<tr>
<td></td>
<td>C7 (&gt;8,300V)</td>
</tr>
</tbody>
</table>

Note: The Above classes may be divided into subclasses

Table 5. ESD testing

<table>
<thead>
<tr>
<th>Test Type</th>
<th>ESD Model</th>
<th>Test Locations</th>
<th>Functional Level</th>
<th>ESD Hardening Requirement</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct contact, non-operating</td>
<td>Body/finger or hand/Metal HBM</td>
<td>Inputs, outputs and interface connections*</td>
<td>All assemblies</td>
<td>2,000 volts</td>
</tr>
<tr>
<td>Direct contact, operating</td>
<td>Hand/Metal HBM</td>
<td>Operator accessible controls and the center of each plane surface</td>
<td>Field maintained equipment</td>
<td>4,000 volts</td>
</tr>
<tr>
<td>Indirect contact, operating</td>
<td>Furniture Model</td>
<td>Horizontal Coupling Plane (HCP) or Vertical Coupling Plane (VCP)**</td>
<td>Digital office equipment</td>
<td>15,000 volts</td>
</tr>
</tbody>
</table>

Notes:

* Inputs, outputs and interface connection points are those points where the assembly is electrically connected to items external to it

** The HCP (or VCP) is a horizontal (or vertical) metal plate that is capacitively coupled to the equipment, to which pulses are applied to simulate discharges to objects adjacent to the equipment
7. Mechanical interface parameters

Mechanical interface parameters related to mechanical interactions between elements, or between an element and its higher level subsystem are described herein. Where illustrative, test methods and test conditions are described. Non-system-level, mechanical interface parameters are defined in IEEE Std. 1515-2000. Annex C, Table C-4 is the directory to the location of mechanical interface parameters described in either this recommended practice or IEEE Std. 1515–2000.

7.1. Packaging

Packaging is defined as the physical characteristics of an element. This includes: physical dimensions, weight, density, materials, potting, sealing, etc described by dimensional drawings, identification of connectors, thermal performance data, and generic package identification.

Note that the distinction between component, Card/CCA, and assembly is made in this recommended practice to facilitate definition of electrical and mechanical interface parameters for different assembly levels of electronic power subsystems. Packaging examples are shown in Figure 17.

![Packaging Examples](image)

Figure 17. Component, CCA, and assembly packaging of electronic power subsystems

7.1.1. Component

A component is a single low-level replaceable circuit element. Components may be discrete items such as resistors or capacitors (passive components), MOSFETs or integrated circuits (active components), or they may be constructed from multiple sub-components such as hybrid circuits, or MCMs (Multi Chip Modules).

7.1.2. Circuit card assembly

A card or Circuit Card Assembly is a power electronic element in a subsystem that consists of individual passive and active electronic components and power electronic elements such as dc-dc converters. The card or assembly may include one or more a daughter board(s) that also can consist of passive and active electronic components.

7.1.3. Assembly, chassis, enclosure, box, rack

An assembly, chassis, enclosure, box or rack is a power electronic element consisting of multiple cards or CCAs and or other assemblies within an enclosed housing. Such elements may be a replaceable part of a larger assembly or a standalone module.

7.2. Center of gravity

7.2.1. Definition

The center of gravity is the physical location within an element for which the mass in all three planes (X, Y, Z) is centered.
7.2.2. Test method

Use a clamping device of suitable size for the element being measured and a mechanism to allow the element to rotate freely. Position the clamp near the apparent center of the element and tighten. Rotate the element about the clamping device and allow the element to come to rest naturally. Once at rest, loosen the clamping device and reposition the clamp on the element at a point lower than the initial position. Repeat this process until the element is positioned in the clamp such that when rotated and allowed to come to rest naturally, the resulting at-rest position is random. Analytical methods for locating the CG of a physical object are well established. Repeat the procedure for the remaining planes to be measured.

7.3. Cooling or thermal energy dissipation process

The cooling process is divided into general methods involving either various means of conduction or electromagnetic wave radiation emission to dissipate the heat generated by a power system. Radiation is in the infrared spectrum. In either method, heat flows from regions of higher energy density to regions of lower energy density.

7.3.1. Thermal interface

A thermal interface is normally a junction where there is a physical break along with a change in the conductive material type in a heat flow path. This interface is sometimes considered the thermal dissipation point of a heat source. This interface may have various physical configurations ranging from the radiation into free space or a vacuum to a conduction path via a "hard" solid cemented or brazed junction.

7.3.1.1. Conduction cooling

Conduction cooling implies the use of a solid physical junction, but also includes heat transfer through any solid, liquid, or gaseous medium.

7.3.1.1.1. Solid physical junction

In this case, heat flows from the dissipating region, normally through a planar surface, across a junction between two solids. The materials involved may be the same, for example when two pieces of aluminum are in thermal contact as part of a heatsink, or they may be different.

7.3.1.1.2. Convection cooling

Convection cooling normally involves a junction between a solid material conducting heat from the dissipating region to a free gaseous or liquid medium in the heat flow path. The most common gas in such power system heat transfer interfaces is atmospheric air. Convection cooling normally implies the use of a “free” or unforced medium, flowing as a consequence of the heat exchange process.

7.3.1.1.3. Forced gas or liquid cooling

Higher rates of heat transfer (greater cooling rates) can be achieved using a means of forcing or pumping the cooling media across or through the interface to the heat source. This is owing to providing a greater number of molecules, some times refered to as the mass flow rate, to carry the heat at a faster rate than free convection.

7.3.1.2. Radiation cooling

Radiation cooling involves the transfer of heat from a dissipating region by electromagnetic radiation in the infrared spectrum. Unless the temperature difference is relatively high between the radiating surface and the heat absorbing surface, the rate of heat flow is not very high. However, this is the only way to dissipate heat in (free) space.

7.3.2. Temperature rise

Temperature rise is the increase in temperature at a point of interest when the power subsystem is in operation as compared to the temperature at the same point when the power subsystem is not operating (and has been shut down for a long enough time to fully cool down). Normally the temperature rise is measured after the power subsystem has been in operation long enough to reach thermal equilibrium.
7.3.3. **Maximum inlet temperature**

Maximum inlet temperature is the maximum allowable temperature of the cooling medium, at the point where it enters the power subsystem, required to maintain the power subsystem elements within their safe operating temperature range.

7.3.4. **Flow rate**

Flow rate is the amount of coolant flow, measured in volume or weight, per unit time. Air cooling is usually measured in volume flow (frequently in cubic feet per minute, or CFM). Liquid cooling is usually measured in weight/mass flow per minute. In and around equipment enclosures, such as VME chassis', a linear flow rate (frequently in linear feet per minute, or LFM) is used to quantify airflow.

7.3.4.1. **Airflow**

Airflow normally refers to the flow of atmospheric air used as the conduction medium at a heat flow junction. It may be referred to both as occurring in a supply duct or as the air passing over the heat exchange junction.

7.3.4.2. **Liquid cooling (closed system)**

Liquid cooling is usually used in applications generating more heat per unit area than airflow systems can remove. Liquid cooling is more complex than air heat exchange because it requires a closed system to conserve the coolant. A liquid coolant should not corrode metal parts, attack rubber, become viscous at low temperature, nor evaporate readily at ordinary module operating temperature.

7.3.4.3. **Pressure drop/back pressure**

Pressure drop/back pressure is the difference in pressure between inlet and outlet coolant flow; that is an indication of coolant flow. It is a consequence of fluid dynamics principles and is affected by heat being dissipated. Pressure drop is also a method for measuring coolant flow rate. The difference between coolant inlet pressure and coolant outlet pressure can be converted to weight or volume per minute using established rules of fluid dynamics.

7.3.5. **Heat pipe (phase change)**

Heat pipes are simple devices that can quickly transfer heat from one point to another, due to their extraordinary heat transfer capacity and rate with almost no heat loss.

A heat pipe is a heat transfer subsystem consisting of a sealed, usually metallic pipe-like container whose inner surfaces have a longitudinal capillary wicking material. The wick capillaries provide the ability to transport heat against gravity using an evaporation-condensation cycle of the heat-carrying medium. The wick capillary driving force returns the condensate from the heat-dissipating end to the evaporator at the heat source. The quality and type of wick usually determines the performance of the heat pipe. Different types of wicks are used depending on the application for which the heat pipe is being used.
8. Environmental interface parameters

Environmental interface parameters concerning a subsystems’ local conditions such as temperature, humidity, vibration, and dust are described herein. Where illustrative, test methods and test conditions are described. Environmental interface parameters usually considered at the element level are defined in IEEE Std. 1515-2000. Annex C, Table C-5 is the directory to the locations of environmental interface parameters described in either this recommended practice or IEEE Std. 1515–2000.

8.1. Thermal

Electronic components operate properly if kept in their safe storage and operating temperature ranges. Even when a component is kept in its safe temperature range, its performance may depend on operation within a preferred temperature sub-range beyond which the component might continue to operate but at diminished performance.

8.2. Resistance to contaminants

8.2.1. Definition

Resistance to contaminants is the capacity of a given substance, usually a solid physical structure or surface, to maintain its properties in the presence of a given material (contaminant).

8.2.2. Test method

The UUT is exposed to the contaminant as required, usually one or more times per day or total immersion, for the specified duration. Following the required exposure, the UUT will be required to operate, under specified conditions, for a minimum time. Alternatively, there may be a requirement that the UUT be placed in a temperature-controlled chamber, for a minimum time period, to evaporate the test fluid before the UUT is required to operate. These tests determine whether the materials used in the construction of the UUT under test can withstand the deleterious effects of the given test substance (generally some type of fluid). The substances will be specified in relevant requirement documents. These substances usually include corrosive agents, solvents, jet fuel, hydraulic fluid, de-icer, etc. These tests are usually only performed when the UUT will be installed in areas where material contamination could be commonly encountered.

8.2.3. Test condition

The types of contaminant, temperature, conditions of the contaminant, and duration of the exposure will be specified.

8.3. Sand and dust

8.3.1. Definition

Sand and dust is sometimes airborne, generally solid particulate matter, both organic and non-organic, usually smaller than 0.005 inch in its major dimension. UUT environmental issues range from simply clogging or fouling airflow paths to providing a medium for abrasion or various corrosive actions. Catastrophic failure can occur due to overheating, clogged passages, or open or short circuits cause by undesired accumulation of material. This test determines the ability of the UUT to resist the effects of blowing sand and dust carried by air movement. Potential adverse effects include, but are not limited to: the formation of electrically conductive bridges, collection of water vapor which could result in secondary effects such as corrosion, and penetration into cracks, crevices and joints resulting in fouling of moving parts such as relays, switches, bearing surfaces, filters, etc.

8.3.2. Test method

The UUT is generally subjected to a sand and dust jet along each direction of each major orthogonal axis in succession using a suitable test chamber. The velocity of the jet will be maintained within specified requirements (determined by the test specification used). At the end of the exposure period(s) the UUT shall be removed from the test chamber and allowed to stabilize to room temperature. External accumulation of sand and dust can generally
only be removed by brushing or wiping and not by air blast or vacuum cleaning. After removal of excess sand and dust, UUT performance is verified by compliance to applicable UUT performance standards.

8.3.3. Test condition
The particle size (generally less than 0.005 inch in its major dimension), particle composition (generally 97 to 99% silicon dioxide), jet velocity (generally between 0.5 and 2.5 m/sec), relative humidity and temperature conditions will be specified during exposure. More than one exposure, at different temperatures for example, may be required. The UUT is usually not required to operate during the exposure period unless otherwise specified. Since many of the test contaminants may have flash points within the test temperature range, or may be toxic, appropriate safety measures should be taken to limit the possibility of fire, explosion or exposure.

8.4. Explosive atmosphere

8.4.1. Definition
An explosive atmosphere is ambient free space containing some manner of combustible, normally "airborne" material along with air or other oxidizer, that is susceptible to being ignited with an explosive consequence. The combustible material may be particulate, aerosol, or gas; this material will normally be the "fuel" in an oxygen or air mix. Electronic power elements may be required to operate in an explosive atmosphere without acting as an ignition source.

8.4.2. Test method
This test can be applicable to normal or fault conditions that could occur in areas that may be subjected to flammable fluids or vapors during operation. The UUT will generally be determined to be explosion proof when it has been determined that there is negligible risk that the UUT will cause an explosion of flammable gas or vapor within the specified environment.

During test, the UUT is placed in an appropriate chamber. An explosive mixture will be maintained within the chamber at the defined mixture, internal pressure, and ambient chamber temperature. In some tests an internal ignition source (such as a spark gap) shall be energized within the UUT case in order to cause an explosion within the case of the UUT. The occurrence of the explosion will be verified by some externally observable method such as a thermocouple used to sense temperature variation. A minimum specified number of internal case explosions will be performed. If the internal case explosion(s) result in a test chamber explosion, the UUT will have failed the test. For less stringent requirements the internal ignition source is not used and it is only required that electrical contacts within the UUT be actuated.

8.4.3. Test condition
Test conditions will vary depending on the type of environment in which the UUT is expected to operate. If the specified environment of the UUT contains uncovered flammable fluids or vapors, the UUT must meet standard and test that are more stringent than if the flammable mixtures occur only as the result of spills or leaks.

8.5. Acoustics
Electronic power subsystems can be the source of acoustic noise (undesirable audible emissions) due to resonance in transformers and other electro-mechanical parts or due to the need to use fans or incorporate cooling passages. Subsystem susceptibility to acoustic noise should also be characterized. The standards governing acoustic noise emission and susceptibility are for physical device safety as well as human safety reasons. These include ANSI S12.35/ ISO 3745; ANSI S12.34/ISO3744; ANSI S12.10/ISO 7779, ASTM C423/ISO 354 and ECMA 74; etc.

8.5.1. Acoustic susceptibility

8.5.1.1. Definition
Acoustic susceptibility is the tendency for a physical or physically induced, usually performance-reducing, effect on subsystem performance due to exposure to a vibration in the acoustic frequency range. This vibration may be structure borne or imposed by a fluctuating gaseous pressure.
8.5.1.2. Test method
Per ISO 354, position the UUT in the reverberation room and measure both sound absorption and total power at the UUT.

8.5.1.3. Test condition
A reverberation chamber is used and the device is properly placed relative to the sound source according to ANSI S12.31.

8.5.2. Acoustic emissions/audible noise

8.5.2.1. Definition
Acoustic emissions are the generation of fluctuating gaseous pressures in the audible frequency range normally due to a physical movement of one or more components of some equipment and subsystem or apparatus. Cooling medium movement may generate audible noise in turbulent flow or when subjected to a change in direction.

8.5.2.2. Test method
Per ANSI S12.31 or ISO 3741.

8.5.2.3. Test condition
Use module as source of noise per ANSI S12.31 performing the measurement in a certified vibro-acoustic laboratory in a calibrated anechoic chamber.

8.6. Radiation
This subclause addresses Nuclear Radiation Effects on electronic power subsystems. Nuclear Radiation herein will be referred to as radiation. Radiation is the propagation of energy through space or through materials. The radiated energy is the emission and propagation of waves or particles. Passage of the radiation through matter creates ionization (charge carriers in insulators) or displacement damage (defects in atomic structure). Both radiation effects lead to performance degradation of the semiconductor device.

There are four major radiation environments that can cause concern with respect to the use of semiconductor devices: total ionizing dose, transient radiation effects (dose rate), single event effects, and neutron radiation.

8.6.1. Total ionizing dose

8.6.1.1. Definition
Total Ionizing Dose (TID) is the amount of the radiation accumulated by the irradiated material normally expressed in Krads (Kilo Rads). The total amount of absorbed radiation energy varies according to the absorption material. The total dose environment can include a composite of gamma rays, X-ray radiation, and other ionization radiation. TID causes a long-term degradation of the semiconductors, which include parametric failures (variations of the voltage thresholds, leakage currents, power consumption, etc) or functional failures in which case the device is not able to perform the intended function(s).

8.6.1.2. Test method
In most cases, a total-dose radiation test plan follows MIL-STD-883E Test methods 1019.4 and 1019.5 requirements. Radiation sources for total-dose testing include X-rays, Gamma rays (Cobalt-60, Strontium-90, Cesium-137), electrons and protons. Each type of source affects the UUT differently, depending on the source’s energy. The most common source for radiation testing is Cobalt-60. The most common system for total-dose measurement is the Thermo-Luminescent Dosimetry (TLD). The American Society for Testing and Materials (ASTM) approved a standard for TLD use in radiation testing, ANSI/ASTM E668-78. This standard specifies using the dosimetry to calibrate gamma-radiation fluence within 10% accuracy at each position from the source, and the calibration must be traceable to the National Bureau of Standards.

8.6.1.3. Test conditions
Test conditions will vary depending on the type of environment in which the UUT is expected to operate. Test conditions are stated in an individual Radiation Test Procedure developed from the Radiation Test Plan. This test
procedure defines the following test conditions: total dose and dose rate for each exposure, ambient temperature (usually 25°C), bias-circuit diagrams showing locations of all circuit elements during each measurement, whether the test is to occur in-flux (during irradiation), required device parameter measurements, and operating conditions during those measurements.

8.6.2. Dose rate

8.6.2.1. Definition
Dose Rate (Transient Irradiation or Gamma Dot) is the amount of ionizing radiation exposure per unit of time normally expressed in rads/sec. Transient irradiation is associated with nuclear explosion and is characterized by a narrow pulse width (usually 3ns - 10µs) containing a total dose of 1000 rad (Si) or greater. A dose rate pulse will generate excess charge in a short period of time. Adverse effects of transient irradiation include upset (soft error), latch-up, junction burnout, short transient pulse on the output, and saturated outputs, which depend on the amount of photocurrent (excess charge) generated and the output loading.

8.6.2.2. Test method
Dose-rate testing normally employs a pulsed linear accelerator (LINAC) or Flash X-ray machine. MIL-STD-883E Test methods 1020 and 1021 outline military dose-rate test requirements. MIL-STD-883E test methods are very well established in the electronics industry. However, other test methods can be used if proven more appropriate for the application.

8.6.2.3. Test conditions
Test conditions will vary depending on the type of environment in which the UUT is expected to operate, and are stated in an individual Radiation Test Procedure developed from the Radiation Test Plan. It is recommended that test conditions used for testing similar products be reviewed before developing new test conditions.

8.6.3. Single event effects

8.6.3.1. Definition
Single Event Effects (SEE) represent the ionizing radiation response of a semiconductor device caused by the impact of individual galactic cosmic rays (electrons, protons, alpha particles, and heavy ions), energetic neutrons and protons. Linear Energy Transfer (LET) is a measure of the energy deposited in a given material by an energetic particle, in electronic collisions per unit length of its trajectory through the material. The LET unit is MeV/ cm²/mg. Radiation responses can include non-destructive effects (upset, multiple-bit upset, etc) or destructive effects (latch-up, gate rupture, burnout).

8.6.3.2. Test method
SEE testing is conducted with heavy ions or protons. The device under test is placed in the beam line of a cyclotron or particle accelerator. Military standard test methods for SEE testing have not been developed, so there is no MIL-STD yet. However, heavy ion testing can be conducted according to the ASTM Test method F-1192M-95. Ambient temperature can have great effect on SEE test results.

8.6.3.3. Test conditions
Test conditions will vary depending on the type of environment in which the UUT is expected to operate, and are stated in an individual Radiation Test Procedure developed from the Radiation Test Plan. Operational testing and temperature are important test conditions.

8.6.4. Neutron radiation

8.6.4.1. Definition
Neutron radiation is emitted during the fission and/or fusion processes. Neutron radiation is a particle radiation consisting of neutrons, leading to defects in atomic structure of the material (displacement damage). The extent of the displacement damage is determined by the neutron fluency normally expressed in neutrons/cm². Atomic structure defects affect lifetimes and carrier mobility, which cause degradation or possible failure of the semiconductor device. Bipolar products are most susceptible to displacement damage due to the importance of carrier lifetimes in the transistor base region.
8.6.4.2. Test method
The irradiation source for neutron testing is a nuclear reactor. Neutron testing normally requires reactor calibration to a 1-MeV equivalent spectrum. MIL-STD-883E Test Method 1017 specifies neutron damage test requirements for military systems.

8.6.4.3. Test conditions
Test conditions will vary depending on the type of environment in which the equipment is expected to operate, and are stated in an individual Radiation Test Procedure developed from the Radiation Test Plan. MIL-STD-883E Test Method 1017 requires that neutron irradiation to be conducted at 25°C and maximum supply voltage.
9. System effectiveness interface parameters

System effectiveness interface parameters include reliability, logistics, and methods to predict or extend the operating life of a subsystem. Where illustrative, test methods and test conditions are described. System effectiveness interface parameters at the element level are defined in IEEE Std. 1515-2000. Annex C, Table C-6 of this document is the directory to the locations of System effectiveness interface parameters described in either this recommended practice or IEEE Std. 1515–2000.

9.1. Qualification requirements

Qualification requirements are the methods used to determine that a product meets its specification requirements. Qualification may be performed by one method or a combination of methods, including similarity, inspection, demonstration, analysis, or test.

9.1.1. Qualification by similarity

Qualification by similarity is when the considered element is determined to be similar in characteristics and exhibited behavior to an element that is fully characterized. Qualification data for the fully characterized element can be used to qualify the element being considered.

9.1.2. Qualification by inspection

Qualification by inspection is when the considered element is measured, weighed, or otherwise observed to determine its characteristics.

9.1.3. Qualification by demonstration

Qualification by demonstration is when the considered element is put into operation and its performance is observed to determine its characteristics.

9.1.4. Qualification by analysis

Qualification by analysis is when the considered element will be analyzed to determine its characteristics. Analysis methods and analysis stimulus available will be known to correlate to previous test data.

9.1.5. Qualification by test

Qualification by test is when the considered element is subjected to approved qualification test(s). Test data will be obtained to show compliance with requirements.

9.2. Quality assurance

Quality assurance is a documented, systematic procedure to ensure that material, process, and test used in the design and manufacture of a product is controlled so that qualification requirements are addressed.

9.2.1. Derating

Derating is the practice of operating components below their rated operating limits to extend their useful life or reliability. Derating is usually stated as a percentage of rated operating limits.

9.2.2. Component quality

Component quality is the level of conformance to requirements as indicated by defect rate, e.g., defective parts per million (ppm).

9.2.3. Screening

Screening is testing element performance according to a statistical test plan.
9.3. Acceptance testing
Acceptance testing is a functional test of the product to requirements.

9.3.1. Test equipment calibration and standards
Test equipment calibration and standards are procedures to ensure the accuracy of test equipment used to verify element compliance to design or performance specifications. Typically calibration requirements include a calibration schedule, equipment calibration standards, requirements for calibration logs and equipment stickers, and instructions for handling product that was found to have been certified with out of calibration test equipment. The calibration services of the National Institute of Standards and Technology (NIST) might be required for validating certain test equipment. (See http://www.nist.gov/ for more information.)

9.4. Compliance information
Compliance information is a list of agency accreditation(s) including any limitations to the accreditation that is required for an element to be approved for use. Examples of organizations that approve certain elements are UL (Underwriters Laboratories), product safety, and the FCC (Federal Communications Commission), regulation of the allocation and use of Radio Frequencies as well as certification of electronic devices for EMI/EMC. Regulatory agencies often require accreditation for equipment before it can legally be offered for public use.

9.5. Logistics
Logistics includes activities required to keep a subsystem operational such as maintenance, provisioning spares, and training of operational and maintenance personnel. Logistics begins during the design stage of a subsystem and continues as long as the subsystem is supported.

9.5.1. Product life
Product life is the expected life of an electronic power subsystem statistically calculated for specified maintenance and operating conditions. Maintenance includes replacement of short life components and repair or replacement of failed sub-assemblies as required. Product life is limited by two main factors: first, the physical life of the hardware, and second the availability of spare parts and maintenance information. These two aspects can be separately defined, as follows.

9.5.1.1. Definition
Useful product life is the length of time over which replacement components can be economically procured, and over which support information and compatible infrastructure are available.

9.5.2. Physical product life

9.5.2.1. Definition
Physical product life is the length of time over which the physical/electrical integrity of the product can be maintained, under normal operating conditions, before wear-out of non-replaceable items.

9.5.2.2. Test method
The principle of accelerated aging can be used to develop an estimate of the likely life of a product, when valid assumptions are made. The UUT is stressed by operating it well outside normal operating levels in order to shorten the time to failure. Stresses might be applied via one or more of the following parameters: temperature, thermal shock, input voltage, load current, or vibration. It is important not to raise stress levels too high since the objective is to accelerate those factors that would result in actual failures during normal operation, rather than causing new types of failure.

Life of electronic components are normally considered to be approximately halved for each 10°C increase in temperature, so that increased temperature is a simple way of accelerating failures. However, it is important not to exceed the rated temperature of components during the test. As an example, if the normal operating temperature is 25°C, but all components in the product are capable of operating up to 85°C, the operating life at 25°C could be accelerated by a factor of 64 by testing at 85°C (60°C temperature increase = x 2^6).

Human factors must also be taken into account, since they may substantially affect life. For example, wear and tear during maintenance may eventually damage parts of a system not considered as repairable, such as the main
framework, shelf structure, system backplane, etc. This type of failure will not be simulated by increasing temperature or other stress factors, but its effect could be estimated by experience with similar previous systems or by a field trial under controlled conditions.

9.5.2.3. Test condition
Apply the stress factors specified for the test and observe the predicted failure(s) if any, since failure does not always take place. The environment for the tests and the conditions under which tests take place is in accordance with prescribed test methods, and the tests are to conducted according to documented procedures.

9.6. Configuration management
Configuration management is a process or system of identification that tracks versions of subsystems. Subsystems may include software, firmware, and hardware assemblies. Configuration management may include record keeping by part, production run, or other relevant grouping.

9.7. Obsolescence
Obsolescence is the occurrence of an “unavailability” situation created by the loss of the last acceptable manufacturer or source of a product, often created by diminishing market demand.

9.8. Discontinuance
Discontinuance occurs when a manufacturer stops producing a part or product. Often a last time buy is offered before an element’s final production. Discontinuance becomes obsolescence if this is a sole source part and no other manufacturer assumes its production.

9.9. Production line certification
Product line certification is the purview of the manufacturer who through a documented Quality Management (QM) program, review system, and status reporting indicates production lines and products manufactured on them are certified to meet applicable requirements.

9.10. Warranty
A warranty is a legal obligation for a product to perform within its specifications for a specified period of performance. Remedies for failure to perform as warranted are stated.
10. System integration

System integration addresses issues of electronic power subsystems specification and design. It is intended to cover the major specification and design issues and to provide guidance to the designer as to the applicability of commercial items. The designer is encouraged to consult additional information about this subject matter and choose appropriate elements that can provide the best user-level system performance, considering pertinent parameters and system requirements.

There are two aspects to system integration – the integration of elements into fully functioning power subsystems, and the integration of power subsystems into systems. Each level of integration introduces new concerns which did not apply at the lower level, and which may affect any of the four interfaces: electrical, mechanical, environmental or system effectiveness. Interactions between the elements may adversely affect the operation of the power subsystem, or may prevent it meeting its specified requirements. Even when the power subsystem is fully functional, there may be further interactions between the power subsystem and the rest of the system that were not apparent in the power subsystem itself.

This section addresses system integration issues affecting the electrical and system effectiveness interfaces; issues affecting the mechanical and environmental interfaces are discussed in Clause 11.

10.1. System interaction

System interaction considerations are essential to successful subsystem implementation. Electronic power subsystems often use distributed power architecture with one or more stages of power conversion, sometimes including parallel elements in some stages. As discussed in Subclause 5.4, the potential interactions between elements must be fully considered during all phases of the power subsystem development - requirements definition, design and test. Since an electronic power subsystem is an integral part of a system, it interacts with the interfaces of the system. All such interactions must be accounted for through analysis and/or system-level tests.

In addition to the electrical interactions, potential thermal, structural, environmental and reliability interactions must also be considered. (These are discussed further in Clause 11.)

10.1.1. Source impedance and system stability – dc systems

In any dc electronic power subsystem where many dc-to-dc power converters are connected in parallel, the dc voltage input rail may become unstable under certain conditions. The reason for this is that all switching power converters exhibit negative resistance behavior at their input, and the condition for oscillation depends mainly on the source inductance – the higher the inductance the more likely the system will oscillate. Note that the source inductance includes the total (worst-case) inductance of distribution wiring, circuit breakers, the source itself, etc. One method to avoid instability in a system is to add capacitance across the dc power rails. This method may be more effective if some series resistance is added to improve the damping. One option is to add bulk capacitance at a central point, and a second option is to add distributed capacitance throughout the system. The preferred option will depend on the system configuration and requirements, but generally the distributed option is more flexible and may simplify the system design. The value of capacitance needed depends on the source inductance and the effective load resistance, as indicated in Figure 18 below. Any stability problem is most likely to show up at minimum input voltage, since the effective load resistance is lowest at this point. The calculation of the required capacitance value should be made with the lowest input voltage at which the system may operate, even including abnormal input voltage sags below the minimum steady-state value. Sufficient margin should be added to the calculated value to allow for the fact that source inductance is usually not well controlled, and to allow for capacitance variation over the product life.
Re = \frac{V^2_{(min)}}{P_{total}}

C_{(min)} = \frac{L}{(R_e * R_s)}

R_e = \text{effective resistance of load}

C = \text{stability capacitor required}

(includes input C of all dc-dc converters)

**Figure 18. Calculation of stability capacitor**

10.1.1.1. Test method

Set up the complete electronic power subsystem including its normal operating load (system under test - SUT), as shown in Figure 19. Add inductance in series with the input connection from the source, to represent the worst-case wiring inductance (maximum cable length, maximum spacing of go and return cables). Set the source to nominal input voltage.

Monitor the input of the UUT using an oscilloscope. Turn on the source and confirm that the UUT is stable in all its operating modes/states. Reduce the source voltage until the input voltage to the UUT is at the lowest specified value (including voltage drop in the wiring) and confirm that the UUT remains stable.

Apply a transient load to the electronic power subsystem, either (preferably) by removing and re-inserting one card in the system or else by adding a small step load through an electronic load. Observe the resulting transient on the input voltage rail and confirm that it exhibits adequate damping – any oscillation should not last more than one or two cycles before decaying to zero.

10.1.1.2. Test condition

System stability should be tested at maximum load and minimum input voltage. It is usually necessary to exercise the rest of the system through its range of functions to find the worst case operating condition. For electronic power subsystems that include a low input shutdown function, it is also necessary to test below the minimum specified operating voltage to confirm stability down to the point where the electronic power subsystem shuts down.

Tests should be carried out at nominal ambient temperature, and repeated at temperature extremes.
10.1.2. Load sharing and redundancy methods

10.1.2.1. Current sharing methods

When constructing electronic power subsystems from available commercial items it is often desirable to parallel multiple elements for increased current or power rating. The potential for using such solutions is partially determined by the degree and method by which the elements will share supplying the load. This subclause is intended to highlight issues to bear in mind when considering use of paralleled elements, not to provide detailed design implementation guidance.

The methods mentioned could be used for load sharing when one commercial item is not sufficient to carry the power load; they also can be used to introduce redundancies for fault tolerant designs. For a simple redundant system the number of elements used in parallel must be sufficient that if one fails, the remaining elements can carry the full load. More complex redundancy schemes may provide several redundant elements so that even if two or more fail the remaining elements can carry the full load.

The following provides some of the more common current sharing schemes are.

10.1.2.2. Direct parallel connection with no current share signal

Elements connected in parallel without specific current share provisions will typically operate as follows. One element will typically have a regulation set point slightly higher than the remaining elements. This element will take current until its output sags to below the no load regulation point of another element. With good load regulation, this may not occur until the first element reaches current limit. Therefore, this scheme will not work with shutdown or cyclic current limit schemes. Even with elements employing linear (square or fold-back) current limiting, there may be performance problems since one or more elements operate in current limit as the load is increased. As a minimum, the elements must be safe for continuous operation with a predetermined overload.

10.1.2.3. Master/slave schemes

There are three types of Master-Slave current sharing schemes. They are known as dedicated master, rotating master, and automatic master. In the dedicated master scheme, one module is designated (by position in the subsystem or by wiring) to be the master, and its output current is measured, processed, and then distributed as a reference for all other modules in the subsystem (slaves). This scheme provides current-sharing and can achieve stable output voltage regulation, but does not achieve redundancy, since failure of the master will result in system failure.

The rotating master scheme is an enhancement to the master-slave scheme, in that it enhances system reliability by providing multiple masters. Used in conjunction with a control logic system, any unit can be selected to be a master based upon the decision of the logic. A drawback to this scheme is that the output voltage may fluctuate as the control logic changes the master from one unit to another. Additionally, the implementation is somewhat more complex than the dedicated master-slave approach.

The automatic master (democratic) scheme is an improvement over the two previously mentioned schemes. A control function is used to monitor the current output from each module. For example the module with the highest current will be chosen as the master and the control function will then correct the current imbalance remaining in the other modules. This scheme is often preferred to the previous schemes since it provides a single interconnecting share bus and good fault tolerance. It is used widely in practical systems. A faulty or weak module will not affect the sharing of the remaining units, and should the current share bus experience a fault, the modules will continue to operate stand-alone. Additionally, the scheme supports easy additions and modifications to the system. Drawbacks include poor transient sharing performance, possible sharing control failure (instability), and sensitivity of the current share bus to noise.

Best performance for current sharing can be achieved by use of converters with inner control loop. An automatic master/slave scheme can then be implemented by a diode-or’ing scheme to set the current reference level directly and common to each converter. A high degree of load-current sharing is achieved without introducing additional dynamics.

10.1.3. Power conversion and switching frequency stability

There are two basic types of switching converters, fixed frequency and variable frequency. Each one has its own merits and pitfalls. The implications of the different schemes are far reaching, and consequently the designer must be aware of the methods and their effects at the system-level. It should be noted that one method should not be favored over the other until all information is gathered, and examined with regard to the system-level requirements.
Additionally, the designer is urged to obtain and test several different types of modules. Testing must be done under realistic conditions that simulate the system installation, in order to be able to verify the actual performance.

10.1.3.1. Fixed frequency power converters
In this mode of operation, the switching frequency is designed to remain fixed, with some tolerance allowed for initial set-point accuracy and deviations from that set-point due to other effects. Typical factors that will affect a change of frequency include temperature, humidity, aging, variable resistor drift, PWM IC discharge current, etc. Typically, switching power supplies operate at a fixed frequency between a few kHz and a few MHz. A typical tolerance of a commercially available module is +/- 10%, as published. However, under extreme operating conditions, it is possible for deviations to approach +/- 50% over the life of the product. The designer is encouraged to inquire about any analyses that the vendor can supply in regard to the “stability” of the switching frequency since the data sheet may contain “typical” data, and not the worst case scenario. The designer should account for this frequency variation with regard to input and output filtering, component selection, and power dissipation.

10.1.3.2. Variable frequency power converters
In a variable frequency operation, the switching frequency is used as the control variable, and is changed dynamically during line and load changes such that a specific mode of operation is maintained. Many topologies utilize variable frequency to insure that switching occurs according to design specification. Some forms of switching are ZCS (zero current switching), and ZVS (zero voltage switching) that may require the frequency to vary such that the internal switches will only switch under the appropriate conditions. Therefore, one can expect the frequency to vary during operation when either a line change occurs, or a load change occurs. Under static operating conditions, the frequency should remain relatively constant.

10.1.3.3. Synchronization
When several switching converter elements are used together in a power subsystem, there is a potential for beat frequencies between them to cause low frequency fluctuations in noise level at the output. For example, if one converter switches at 300 kHz and a second converter switches at 310 kHz, there will be a small noise component at 10 kHz. In most applications this is not important but for some types of system even a very low level of noise may be detrimental to system performance.

For such sensitive systems, it may be preferable to synchronize the switching frequencies of all elements to ensure they all have the same frequency and avoiding any possible beating. In some cases, it may be necessary to derive the synchronization signal from a critical system clock frequency, to keep power element noise to an absolute minimum. Note that such synchronization is only possible with fixed-frequency converters, and only if the converter element provides a synchronization input.

10.1.3.4. Impact of switching frequency on EMI
All switching converters generate some amount of EMI. There can be large differences in EMI performance due to the chosen switching topologies, and the method of frequency control. The designer is encouraged to solicit information from the vendor, to obtain accurate plots of Differential Mode (DM) and Common Mode (CM) noise on both the input and output terminals. The impact of frequency stability over line, load, temperature, and useful product life should be analyzed.

10.2. Protection and sensing

10.2.1. Overvoltage protection
Overvoltage protection in a converter is a mode of protection that inhibits the converter’s output from going catastrophically high under a fault condition in the voltage feedback loop. Should the voltage feedback to the converter’s control IC fail and provide feedback to the control IC that there is no or low voltage at the output power pins of the converter, the control IC will compensate for this falsely low output voltage feedback signal and cause the output to go much higher than the regulation voltage of the converter. This could cause significant system load damage in the absence of an overvoltage protection circuit. These circuits monitor the output voltage of the converter at its output power pins. The circuits override the voltage feedback signal and inhibit the output voltage from going catastrophically high. Some converters have a latching-shutdown type of overvoltage protection circuit where when activated, the converter will shut down and require removal of the input power prior to the output voltage being restored. Other converters have a non-latching, non-shutdown type of overvoltage protection mode and will continue to operate until the fault condition goes away. Some other converters may have a non-latching,
shutdown type of circuit. This is generally undesirable because the output becomes a square wave whose amplitude
goes from zero volts to the overvoltage trip point, with a period set by the turn-on time of the converter and the
activation time of the overvoltage protection circuit.

10.2.2. Remote sensing

Many converters have an output voltage sensing circuitry available to the user through external output voltage sense
pins. The converter will regulate the output voltage at the point to which these pins are attached. These pins can be
very useful to the user of the converter. For example, a user’s system may have significant impedance in the power
cables that connect the output power pins of the converter to the system load. This impedance can cause the voltage
at the system load to fall below the desired level because of the voltage drop in the power cables. The sense pins can
be connected at the load, thereby causing the converter to regulate at the load rather than at the output of the
converter. This practice is called *remote sensing*. There are some cautions that need to be observed while remote
sensing.

When remote sensing, the power load cables, and sense cables are part of the converter’s voltage feedback loop.
Both the output power load cables and the sense cables should therefore be shielded to minimize noise pickup. The
inductance of the cables should also be kept to a minimum. A good method of connecting the cables is running
parallel planes on opposite layers of a PWB. For example, the plus output voltage signal might be a ½ inch wide
trace on one layer and the minus output voltage signal would be another ½ wide trace on another layer directly
below or above the plus output voltage signal. The sense signals would be routed in the same fashion.

It is also good practice to have an additional ground plane layer between system noise sources and the sense and
load signals. Another good method for connecting the load and sense lines to the system load is to use a ground-
shielded twisted pair.

If achieving low inductance in the sense and load cables is not possible in the user’s system, a capacitor can be
connected from the plus output power pin to the plus sense pin in addition to a capacitor of equal value from the
minus output power pin to the minus sense pin. These capacitors can help offset the parasitic inductance that the
sense cables and power load cables have introduced into the converter’s voltage feedback loop. If employing these
capacitors, the user should be aware of the polarity of these capacitors, as the plus output power pin will be at a
higher potential than the plus sense pin, and the minus sense pin will be at a higher potential than the minus output
power pin. To maximize the effectiveness of these capacitors, they should be connected in close proximity to the
pins of the converter.

Note that it is very important that the OVP sensing is connected separately, rather than to the sense leads, or else
there will be no protection under some of the possible fault conditions discussed below.

10.2.2.1. Open sense leads

One fault condition that can occur while remote sensing is that the sense lines become open-circuited. Because the
sense lines are the source of voltage feedback to the converter, the control IC within the converter is given the signal
that there is no voltage at its output under this condition. Without any open-sense protection, this would cause the
output of the converter to go into an overvoltage protection mode. Open-sense protection is accomplished by
connecting a resistor between the positive output power pin and positive sense pin. Another resistor of equal value
is connected between the minus output power pin and the minus sense pin. The value of these resistors should not
be too small, or the converter will be in effect sensing the output of the converter locally, rather than at the system
load. If the value of these resistors is too large, the converter will still go into overvoltage protection should the
sense lines become open-circuited. A typical value for a converter with a 5V output is 100 ohms for each resistor.

10.2.2.2. Shorted sense leads

Another fault condition to consider is the sense lines becoming shorted while the output power pins are not shorted.
Similar to the case of open-circuited sense lines, the converter’s voltage feedback is sensing that there is no voltage
at the output power pins. This condition will cause the converter to go into an overvoltage protection mode. If
employing the open-sense protection resistors mentioned earlier, the open-sense protection resistors will experience
dramatic increase in the power dissipated. The worst-case scenario power dissipation in these resistors is the
following condition; one of the sense lines becomes disconnected from the load and is shorted to the other sense
line. Again, the converter’s voltage feedback circuitry is sensing that there is no voltage at its output power pins and
the converter goes into an overvoltage protection mode. The open-sense protection resistor that is connected
between the open sense line and the output power pin has the entire output voltage of the converter across it under
this condition. A 5-volt converter may have its overvoltage set point at 6 volts and an open-sense protection resistor
with a value of 100 ohms. This resistor would be subjected to 360mW under this condition. This is significantly
higher than the steady-state power dissipation in the resistor, which would typically be less than 1mW. However, this high level of dissipation only occurs during the short interval before the unit shuts down.

10.2.2.3. Reverse sense leads
Another fault condition that may occur while employing remote sensing is reversed sense lines. Similar to the open-sense and shorted-sense conditions, a converter’s control IC will sense that there is no voltage at its output power pins and the converter will go into an overvoltage protection mode. Having the sense lines reversed may cause permanent damage to the converter, as many converters have polarity sensitive components that are connected across the sense lines.

10.2.2.4. Local sensing
Many users will connect the sense pins directly to the output pins of a converter, thus employing local sensing. In order to keep the voltage at the system load at an acceptable level, the user will trim the converter up to a level that results in an acceptable voltage level at the system load. For example, a 5-volt system may have a 300mV voltage drop in its output power load cables at full load. The user could trim the output of the converter to 5.3 volts, resulting in 5.0 volts at the system load. Of course, the voltage at the system load is then dependant upon the current in the output load cables. In this system, at no load, the voltage applied across the load would be 5.3 volts. The system is simpler, more reliable, and less susceptible to noise, at the cost of inferior load regulation. Some converters allow the user to trim the output by connecting a resistor between two external pins. Other converters need to be trimmed at the factory.

10.3. Output sequencing and clamping
For centralized power systems, the sequence in which output voltages power up is fixed and cannot easily be controlled on individual cards. For distributed power systems, each card generates its own low voltage rails and the sequence can be different on each card. For most systems, the power up sequence between different CCAs (circuit cards assemblies) is addressed at the system-level, by the design of the digital hardware and the system software, and does not need to be addressed in the electronic power subsystem.

For any card using more than one voltage rail provided by on-card dc-to-dc converters, not all rails will appear exactly simultaneously during power-up, and the sequence in which the rails power up may be important. The sequencing requirement of the output voltage rails will depend on the types of components (ICs and ASICs) used in that card, and are becoming more critical as components become more and more complex and supply voltages are reduced.

10.3.1. Output sequencing
Many new components require two voltage rails, one for the ‘internal’ circuits of the component and a different, higher voltage for the I/O circuits and drivers. Many of these components require the lower voltage to be applied before the higher voltage, sometimes with a given time interval between them. If the rails are applied in the incorrect sequence, it may result in latch-up, malfunction, or even permanent damage to the component. The electronic power subsystem must be designed to guarantee that the voltage rails power up in the correct sequence and, in some cases, power down in the reverse sequence. This feature is usually not provided in commercial dc-to-dc modules, but may be added by using different time delays in the enabling of each dc-to-dc converter, or by a logical interactive scheme that requires one output to be present before enabling the other.

10.3.2. Output clamping
Some components are very sensitive to small differences in voltage between supply rails. For cards using these components, some of the output voltage rails may require clamping to limit the voltage difference between supply rails due to a short on the card, or in the event that one dc-to-dc converter fails.

One way to achieve this is to use diodes between rails (using several diodes in series, where necessary) to provide instantaneous protection of the load. The diodes themselves must carry the full output current of the dc-to-dc converter, and can be protected by the undervoltage detection circuit, which will shut down all dc-to-dc power modules on the card.

Clamping may also be needed to protect against overvoltage, again using diodes to prevent the low voltage rails from exceeding the higher voltage rails during transient fault conditions. In addition, the overvoltage detection circuit will shut down all dc-to-dc converters on the card if an overvoltage is detected. One must be cautious that in some cases clamping diodes may have difficulty working with power modules using synchronous rectifiers.
As in the case of sequencing, the exact details will depend on the components used in the circuit.

10.4. Supervisory/status monitoring, control, and software implementation

10.4.1. Status monitoring

Status monitoring is the capability to detect that essential parameters of a power subsystem are within predetermined limits, and to provide an indication if one or more of the monitored parameters is outside the predetermined limits. This may be achieved through a local or a remote monitoring interface. Examples include indication of fuse or circuit breaker state, indication of output voltage or current, indication of battery status, etc. This capability may also provide an indication if a failure is detected in a subsystem or module within the electronic power subsystem, even if performance parameters remain within the predetermined limits.

In general, any electronic power subsystem requires some form of control and monitoring. For a simple electronic power subsystem, the monitoring may be integrated into the power converter module itself, and no separate controller may be required. However, in larger or more complex electronic power subsystems the controller may be implemented as a separate module within the subsystem.

Normally a hierarchical arrangement is used for control and monitoring. Control of operating parameters is achieved at a local level, for example by the use of a PWM control for output voltage, or by the provision of a local overvoltage protection shutdown.

Supervision of each element uses a local controller within the element to monitor output voltage and current, to set operating parameters such as output voltage or current limit, to monitor the status of alarms, and to provide an interface to the system controller.

A system controller is used to monitor operation of the electronic power subsystem, monitor and control each element through its local controller, and provide the electronic power subsystem user interface. The functions provided by the system controller depend on the electronic power subsystem specification and requirements, and may include some or all of the following:

Monitoring functions
- System output voltage(s)
- System output current(s)
- Input voltage
- Input current
- Temperature at one or more points in the system
- Battery status (if applicable)
- Battery charge or discharge current
- Status/failure of modules
- Status/failure of standby elements in redundant system
- Environmental monitoring
- Hold-up time

Control functions
- Adjust output voltage
- Set protection levels for overcurrent
- Set protection levels for over/undervoltage
- Output power sequencing
- Load current sharing between elements
- Remote on/off
- Set protection level for overtemperature
- Configure the power system by enabling/disabling elements
- Remote reset of circuit breakers
- Periodic testing of elements
- External synchronization
User interface functions
- Status of monitored data
- Input parameters for control actions
- Alarm signal to “outside world” (may be local or remote)
- Remote user interface (RS232, modem, web access, MIL-STD-1553b, etc)
- Display information in a convenient and user-friendly manner

10.4.2. User interface example
The user interface may be very simple, such as an indicator light to show presence of input voltage or to show “power good,” or may be more complex to provide more information or more control options.

As an example, consider a typical laptop PC electronic power subsystem. The user interface includes the following aspects:
- An LED on the ac power adapter to indicate presence of ac power (also acts as a failure indicator)
- An LED on the body of the laptop to indicate power ON
- An icon on the display screen indicating battery charge status and presence of ac power.
- A dialog box in Windows to allow user selection of key parameters in the system – time before power down while on battery power, time to power down while on ac power, etc.

To provide these indications, the PC electronic power subsystem includes hardware to monitor dc voltage level and battery charge/discharge current, and must provide hardware control inputs to allow selective powering down of portions of the electronic power subsystem. In the case of the PC, the “system controller” (the microprocessor) controls and monitors the electronic power subsystem through software. The user interface is provided partly by hardware (LEDs) and partly by software generating messages, icons, and charts through the operating system.

10.5. System reliability

10.5.1. Failure modes effects and criticality analysis
Failure modes effects and criticality analysis (FMECA) is a commonly used method for reliability assessment. It is defined as a three-step process:
- Systematically consider all the possible failure modes of a product
- Determine the effect of each failure mode on the performance of the product
- Assess how critical that failure mode is, depending on the likelihood of it occurring as well as the severity of the effect

Reduce or eliminate the most critical failure modes, either by reducing the likelihood of the failure mode occurring, or by reducing the severity of the effect of the failure mode when it does occur.

10.5.1.1. Unit level FMECA
In some cases, it may also be useful to apply the technique of FMECA at component level within a subsystem. Analyzing possible failures of each component may help to identify additional possible failure modes at the subsystem-level. However, this type of FMECA is usually more difficult and time-consuming due to the large number of components in the subsystem. It also requires detailed knowledge of the circuit design and components, and may not be possible when using commercial items.

10.5.1.2. System-level FMECA
FMECA may be carried out at the system-level where the “external” failure modes of each element are considered. For example, for a dc-dc converter element the failure modes may include the following (some of which may occur simultaneously):
- No output voltage, output open circuit
- No output voltage, output short circuit
- Output voltage high
- Output voltage low
- Excessive output ripple
Output unstable  
Input short circuit  
Input open circuit  
Low efficiency (overheating)  
Incorrect switching frequency  
Incorrect monitor outputs (output voltage indication incorrect, output current monitor incorrect, etc., and as applicable)  
Control input failure (remote shutdown failed ON, remote shutdown failed OFF, etc., as applicable)  

The effect of each failure mode will vary widely, depending on the application of the element in the electronic power subsystem, and depending on the application of the electronic power subsystem in the system. Frequently, a so-called “brainstorming” session may be a very effective means to review the design and look for all possible failure modes. Initially, all failure modes can be captured however unlikely they may appear. After the brainstorming, the suggested failure modes are reviewed in more detail and for each failure mode, an estimate is made of the likelihood of this failure mode occurring, and the severity if it does occur. An order-of-magnitude estimate is usually sufficient, and by multiplying the likelihood and severity together, a ranking can be made showing the most critical failure modes. Those failure modes near the top of the ranking will then be reviewed in more detail and actions taken as appropriate. The actions taken to reduce the criticality of a failure mode may address either or both of the following:
- Reduce the likelihood of the failure  
- Reduce the severity of the effect  

The likelihood of failure may be reduced by actions such as:
- Component screening,  
- Component stress derating,  
- Adding environmental relief such as heatsinks or fans to reduce temperature, heaters to remove moisture, damping to reduce vibration effect, etc.  

The severity of the effect of a failure mode may be reduced by actions such as:
- Adding redundant elements,  
- Adding protection elements,  
- Adding special environmental enclosures such as enclosing in a fireproof housing, etc.  

10.5.2. Part stress analysis and parts derating  
Electronic parts can exhibit premature failure due to overstress, especially voltage and thermal stress. Certain parts are more stress sensitive than others are. Reductions in failure rate can be achieved by reducing the stress levels by good design practices. Reducing part stress levels has become well developed and is called “derating.”  
The electronic-electromechanical-electrical parts application analysis shall be performed to verify that the applied stresses on the components at qualification test temperature levels do not exceed the part’s stress derating guidelines. In the analysis, it shall be assumed that the element base-plate is set at the maximum qualification temperature limit; the piece part operating temperature should then be determined by thermal analysis. Note that for elements that do not have a base-plate, maximum ambient temperature should be used for the analysis.  
Derating is the process of designing parts to operate at stress levels below the manufacturer’s rated values. Derating procedures vary with different types of parts and their application [B1] [B2] [B3]. For example, resistors may be derated for power and voltage. Derating is also advisable to provide some margin for analytical error. As most part failure rates are exponentially dependent on temperature, it is obvious that derating to achieve low operating temperature is essential to long life.  
Proper parts derating leads to increased useful life. Derating levels can be verified by current testing, parts stress analysis, past experience, and engineering common sense.  

10.5.3. Worst case analysis  
Worst case analysis (WCA) is an extension of classical circuit analysis using element parameter data and conditions at their extreme values rather than the nominal value. In WCA, the classical circuit analysis is repeated for various combinations of extreme values of element parameters and conditions. The objective of WCA is to verify that the
circuit performs as required for all combinations of allowable and/or observable element parameters and conditions, particularly for those known combinations of maxima and minima towards the end of useful life.

Circuits that are designed to provide the required output at nominal conditions and parameters may not meet the output requirements if the operating conditions or parameters vary from the nominal values over their required range. When several element parameters vary excessively from nominal values, out-of-specification performance is likely to occur. This type of circuit behavior may be predicted using WCA and might lead to design modifications to achieve functionality for specified life cycle or curtailing the life cycle.

10.5.4. WCA methodology

WCA methodology has been developed over the years to address parameter variation effects for both analog and digital circuits. To facilitate the performance of the WCA, complex circuits may be reduced to smaller functional blocks. By using this approach, the analysis becomes more manageable. When a circuit is reduced to these functional blocks, performance requirements for each block input and output should be established. These requirements will serve as the evaluation criteria for the WCA results for each functional block. Some of the requirements for the functional blocks may be derived from higher-level specification requirements. The WCA should show compliance with all requirements, both on the functional block level and at the circuit level. Proof of compliance to certain less significant requirements may be omitted if adequate justification for the specific omission is given.

In many cases (e.g., RF circuits), the modeling and analysis of a circuit may prove to be extremely difficult and questionable for certain parameters. In these cases, it may be expedient to use laboratory test data in conjunction with analysis to determine the worst-case response. For those elements that are difficult to model, the laboratory test is used to establish the sensitivity, which can be used in a simplified analysis to achieve all worst-case conditions.

Performance of a WCA is an effective means for assuring the presence of adequate design margins in electronic circuits. The WCA should be an integral part of the design of every electronic assembly. The analytical results will serve to assure proper operation of the circuit under the most unfavorable combination of realizable conditions or to identify potential performance problems for circuits whose worst-case analytic results show deviation from specified performance requirements. The WCA should be performed as the design evolves, but prior to design freeze.

One of the most important aspects in the WCA is the element parameter variation used in solving the circuit equations. If a design is to pass a WCA, it must be designed with the same worst-case element parameter variations to which it will be subjected in the WCA.

If design changes are made, because of the WCA or for other reasons, the WCA is to be updated using the new circuit. It is important to note that WCA is not a substitute for hardware testing at different levels of integration as required and/or deemed necessary.

10.6. Logistics

Logistics includes activities required to keep a system operational. Logistics is addressed through analysis of those design characteristics that generate a need for, or are associated with, providing support to the total system. Individually, they may be viewed as hardware, software, or support system design characteristics. Collectively, they represent the “supportability” of a total system.

Strategies and requirements to minimize the burden of logistics should be considered throughout the process of electronic power subsystem design and implementation. Processes and goals such as configuration management, reliability assurance, obsolescence management, and planned technology insertion require planning from the beginning of the development process, particularly when considering the use of commercial items in applications with traditionally rigorous logistics requirements such as avionics, military, or space.

Commercial items are normally considered as ‘components’ or elements from a logistics perspective because configuration management will generally not be possible below the component level. At the component level, version control may not be comprehensive. In addition, reliability data, particularly in specific formats or for specific environments, may not be available. However, the subsystem designer or integrator can use methods including Highly Accelerated Life Test (HALT) and Highly Accelerated Stress Screening (HASS) to mitigate these limitations. Reliability predictions can be derived from HALT results through knowledge of the application operating conditions. Quality assurance can be achieved through HASS and/or other screening or sampling test methods. These methods help to assure that internal component or manufacturing process changes, within a subsystem, do not compromise the functional performance or reliability of the subsystem.
Reliability data is often used to determine the provisioning level of spares and to predict uptime availability. In the absence of such data, availability may have to be addressed by a manufacturer’s warranty and repair turn around time.
11. System adaptation

Adaptations can be made to any or all of the system interfaces described in Subclause 5.1. The benefit of adapting a commercial item must be favorable with regard to a custom development considering schedule, risk, performance, and total cost. System integrators need to exercise prudence in implementing adaptations. From a logistics perspective, it may not always be practical to adapt to an interface. Although the benefits of using commercial items often outweigh any associated logistics issues, this should be confirmed. The commercial item vendor should be consulted whenever an adaptation to a commercial item is contemplated.

Various adaptation strategies are described in this clause. These adaptations should be considered suggestions and may not be appropriate for a particular subsystem.

11.1. Electrical interface adaptations

Table 6 indicates possible electrical adaptations of elements when there are interface incompatibilities, and indicates what may be the impact in each case. More commonly used adaptations are indicated in bold. More details on each adaptation are described in the paragraphs following the table, as indicated in the column “reference”.

Whenever an adaptation is being considered as a design option, there are several factors that should be fully taken into account, including the following:

- Not all suggestions are practical in all circumstances
- The adaptation may have an impact on performance
- Detailed design and testing is needed to successfully implement adaptations
- Element designers should be consulted to confirm that proposed solution is appropriate

The total benefits of adapting an existing unit (development cost, unit cost, unit size and weight, time to market, logistics, etc.) should outweigh the cost of alternative implementations.
Table 6. Electrical interface adaptations

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ac input voltage mismatch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Steady state</td>
<td>Add step up or step down transformer in front of unit</td>
<td>Additional space, weight, reduced efficiency</td>
<td>11.1.1.1</td>
</tr>
<tr>
<td>Overvoltage spike</td>
<td>Add transient suppressor</td>
<td>Minimal</td>
<td></td>
</tr>
<tr>
<td>Overvoltage transient, long</td>
<td>Add special transient suppressor or circuits</td>
<td>Additional space, efficiency</td>
<td></td>
</tr>
<tr>
<td>duration</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage spike</td>
<td>Add more output holdup capacitors</td>
<td>Additional space, may require access to node internal to element</td>
<td></td>
</tr>
<tr>
<td>Undervoltage transient, long</td>
<td>Add more output holdup capacitors, use oversized supply, or use step up</td>
<td>Additional space, may require access to node internal to element, step up transformer may</td>
<td></td>
</tr>
<tr>
<td>duration</td>
<td>transformer in front of unit</td>
<td>exceed max input voltage</td>
<td></td>
</tr>
<tr>
<td>Dc input voltage mismatch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Steady state</td>
<td>Add step up (boost) or step down (buck) transformer in front</td>
<td>Additional space, efficiency</td>
<td>11.1.1.2</td>
</tr>
<tr>
<td>Overvoltage spike</td>
<td>Add transient suppressor</td>
<td>Minimal</td>
<td></td>
</tr>
<tr>
<td>Overvoltage transient, long</td>
<td>Add special transient suppressor or circuits</td>
<td>Additional space, efficiency</td>
<td></td>
</tr>
<tr>
<td>duration</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage spike</td>
<td>Add more input holdup capacitors</td>
<td>Additional space, efficiency</td>
<td></td>
</tr>
<tr>
<td>Undervoltage transient, long</td>
<td>Add more output holdup capacitors, or Use oversized (in power) unit</td>
<td>Additional space, efficiency</td>
<td></td>
</tr>
<tr>
<td>duration</td>
<td></td>
<td>Oversized unit may not meet holdup requirement</td>
<td></td>
</tr>
<tr>
<td>Dc power element with ac input</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>source</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>100-200V dc input unit with</td>
<td>Add full wave ac input rectifiers and filtering capacitors</td>
<td>Some additional space</td>
<td>11.1.1.3</td>
</tr>
<tr>
<td>115V ac</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200-400V dc input unit with</td>
<td>Add half wave voltage doubler rectifier and filtering capacitors</td>
<td>Some additional space</td>
<td></td>
</tr>
<tr>
<td>115V ac</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>200-400V dc input unit with</td>
<td>Add full wave ac input rectifiers and filtering capacitors</td>
<td>Some additional space</td>
<td></td>
</tr>
<tr>
<td>230V ac</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>36-72V dc input unit with 115V or</td>
<td>Add conversion stage, optionally with PFC</td>
<td>Additional space</td>
<td></td>
</tr>
<tr>
<td>230V ac</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Table 6. Electrical interface adaptations (continued)

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input current does not meet EMI/EMC requirement</td>
<td>Add EMI filter(s) in front to meet regulatory requirements:</td>
<td>Minimal</td>
<td>11.1.1.4</td>
</tr>
<tr>
<td></td>
<td>Commercial products (USA) must meet FCC Rules and Regulations, Title 47, Part 15, Subpart J [B12]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Military products (USA) must meet MIL-STD-461 [B10]</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Commercial products (non-USA) – requirements vary but are generally in line with FCC [B12] or CISPR 22 [B13]</td>
<td></td>
<td>11.1.9.2.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Systems, including the electronic power subsystem, should be analyzed and must be tested for all mandated EMI/EMC requirements and regulations</td>
<td>11.1.9.2.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>11.1.9.2.3</td>
</tr>
<tr>
<td>Input power factor does not meet requirements</td>
<td>Add power factor correction conversion</td>
<td>Additional space, reduced efficiency</td>
<td>11.1.1.5</td>
</tr>
<tr>
<td>Open mismatch</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage in between standard output voltages available</td>
<td>Use a higher output element and trim down the output voltage to required value, or</td>
<td>Minimal</td>
<td>11.1.1.6</td>
</tr>
<tr>
<td></td>
<td>Use two different output voltage elements in series</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Other special voltages</td>
<td>Use two or more, same of different, output voltage elements in series</td>
<td>Space, compromised performance</td>
<td></td>
</tr>
<tr>
<td>Output ripple voltage too high</td>
<td>Additional filtering capacitors or additional LC filter</td>
<td>Some additional space</td>
<td></td>
</tr>
<tr>
<td>Required current higher than supplied</td>
<td>Parallel two or more identical elements</td>
<td>Normal practice (Caution – some elements cannot operate in parallel)</td>
<td></td>
</tr>
<tr>
<td>Input protection</td>
<td>Place a diode in series with the lead so that the reverse current is blocked</td>
<td>Reduced efficiency</td>
<td>11.1.2.1.1</td>
</tr>
<tr>
<td></td>
<td>Place a reversed-biased diode across the input of the power supply</td>
<td>Need to trip input fuse or circuit breaker</td>
<td>11.1.2.1.2</td>
</tr>
<tr>
<td>Input undervoltage protection</td>
<td>Monitor the input voltage and shut down or disconnect if it falls below its rated minimum</td>
<td>Minimal</td>
<td>11.1.2.2</td>
</tr>
<tr>
<td>Input overvoltage protection</td>
<td>Monitor the input voltage and activate an overvoltage protection circuit in an overvoltage condition</td>
<td>Added complexity. Requires some space</td>
<td>11.1.2.3</td>
</tr>
<tr>
<td>Input transient suppressors</td>
<td>Utilize TVS diodes in series to obtain higher standoff voltages</td>
<td>Normal practice</td>
<td>11.1.2.4.1</td>
</tr>
<tr>
<td></td>
<td>Utilize parallel-connected TVS devices to increase power rating</td>
<td>Normal practice</td>
<td>11.1.2.4.2</td>
</tr>
</tbody>
</table>
### Table 6. Electrical interface adaptations (continued)

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output protection</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output overvoltage protection</td>
<td>Add a monitor circuit and OVP</td>
<td>Minimal</td>
<td>11.1.2.5</td>
</tr>
<tr>
<td>Output good signal</td>
<td>Add a window detector (normally two comparators)</td>
<td>Need to design carefully to avoid nuisance trips</td>
<td>11.1.2.6</td>
</tr>
<tr>
<td>Output current protection</td>
<td>Add overcurrent protection circuit</td>
<td>Need to determine whether to use latch-off or “hiccup” circuit (to maintain compatibility with other elements)</td>
<td>11.1.2.7</td>
</tr>
<tr>
<td>Power system fault protection</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Insufficient fault protection in power elements requires protection at subsystem level</td>
<td><strong>Add protection elements where needed within the power subsystem</strong></td>
<td>Protection elements must be correctly sized so that under the fault condition the intended element opens and other elements do not open</td>
<td>11.1.2.7.3.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Each protection element must be rated to handle the maximum fault current</td>
<td>11.1.2.7.3.2</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transients due to protection element operation must be considered</td>
<td>11.1.2.7.3.3</td>
</tr>
<tr>
<td>Input indication</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Indicator circuits for ac inputs</td>
<td>For single or three phase inputs, an opto-coupler or transformer could be used to monitor the phase-to-phase or phase to neutral voltage. For three phase systems, a delta configuration of opto-couplers can be used to determine if one phase has dropped out</td>
<td>Normal practice</td>
<td>11.1.2.8</td>
</tr>
<tr>
<td>Indicator circuits for dc inputs</td>
<td>An opto-coupler or oscillator may be used as a threshold indicator</td>
<td></td>
<td>11.1.2.9</td>
</tr>
<tr>
<td>Stability</td>
<td><strong>Add capacitance if necessary to ensure stability</strong></td>
<td>The integration of multiple standard elements requires analysis to prove that the system will remain stable</td>
<td>11.1.3</td>
</tr>
<tr>
<td>Electrostatic discharge</td>
<td>All components of a system must be designed for and protected against ESD effects according to system requirements (for example, an Electrostatic Discharge Control Program such as MIL-STD-1686 Rev C [B8])</td>
<td>At the subsystem-level this can involve careful positioning of elements, and may require additional shielding. At the element level, it also requires consideration of circuit design details and PCB layout</td>
<td>11.1.5</td>
</tr>
</tbody>
</table>
## Table 6. Electrical interface adaptations (continued)

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isolation and grounding issues</td>
<td>Electrical isolation is obtained through transformer isolation, optical isolation, and or protection device isolation</td>
<td>Must be fully considered at element and subsystem level. The electronic power subsystem must not compromise grounding requirements for the system</td>
<td>11.1.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Normal practice</td>
<td>11.1.6.2</td>
</tr>
<tr>
<td>Electrical terminations</td>
<td>Use a suitable interconnect assembly with the appropriate connectors for each element and for the system interconnection interface</td>
<td>Elements with fixed switching frequency are preferred for low noise applications</td>
<td>11.1.7</td>
</tr>
<tr>
<td>Output noise due to varying switching frequency of an element, or beat frequency between elements</td>
<td>When determining the applicability or suitability of specific elements, need to balance the noise output versus the expected change in frequency.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output does not meet EMI/EMC requirement</td>
<td><strong>Add EMI filter(s) to outputs, to meet regulatory requirements:</strong> Commercial products (USA) must meet FCC Rules and Regulations, Title 47, Part 15, Subpart J Military products (USA) must meet MIL-STD-461 Commercial products (non-USA) – requirements vary but are generally in line with FCC or CISPR 22</td>
<td>Normal practice Systems, including the electronic power subsystem, should be analyzed and must be tested, for all mandated EMI/EMC requirements and regulations</td>
<td>11.1.4</td>
</tr>
<tr>
<td></td>
<td>Monitoring and control can be performed by the system controller</td>
<td>The aspects which can be monitored are limited to those available at the interface to the element If a commercial item element does not provide a required control capability, it may be possible to implement it externally If software is used, the software must be fully taken into account during the system design and integration</td>
<td>11.1.10.1</td>
</tr>
<tr>
<td></td>
<td>May use a standard data communication link (such as RS232, or CAN) with defined protocol</td>
<td></td>
<td>11.1.10.2</td>
</tr>
</tbody>
</table>

---

8/19/2002

Copyright ©2002 IEEE. All rights reserved.
This is an unapproved IEEE Standards Draft, subject to change.
11.1.1. Input voltage and current

When selecting a commercial item element for a specific application, one of the problems is that the input characteristics of a power element do not match the application’s power source characteristics. To accommodate the difference, a certain adaptation scheme has to be used between the power element and its power source. The following are some examples.

11.1.1.1. Power supply with ac input

The characteristics of most of the ac source are basically categorized as Normal Steady State Limit (NSSL), Abnormal Steady State Limit (ASSL) and Emergency Steady State Limit (ESSL) [Mil Std 704 ref, MIL-STD-1399, Sect 300 [B16]]. Most of the commercial-off-the-shelf power supplies have no problem operating within the high or low side of the NSSL of typical military ac power sources. If the steady state ac input voltage is higher or lower than the input voltage range of the power supply, a step down or step up transformer will be needed to correct the mismatch problem. Some of the commercial power supplies may have a problem operating to the ESSL and most commercial power supplies will have a problem operating to ASSL.

For cost and size reasons, most of the commercial power supplies do not have much reserved capacity. This affects the regulation of the power supply at low input voltage, including the low end of the input range and the low voltage transient. Furthermore, for the same reasons mentioned above, most commercial power supplies have little margin in their components’ derating. This decreases the reliability or the survivability of the power supply at high abnormal steady state input voltage. The ESSL and ASSL low line operation problems can be mitigated by adding more hold-up capacitors at the power supply’s output, or by specifying a power supply that delivers more power than the system requires under worst case condition at low line of the NSSL input operation. This method works only when the power supply’s internal house keeping supply is capable of working down to or below the low side of ASSL. Otherwise, a step up transformer is required electrically ahead of the module.

In general, the overvoltage limit is much harder to adapt to than the undervoltage limit. If the derating margin of the components of the power supply, particularly the semiconductor devices, is not high enough to withstand the worst case ASSL overvoltage, an amplitude limiting circuit has to be used at the input of the power supply. Because of the long duration of the overvoltage during the abnormal operation, the selected amplitude limiting circuit or device must be able to absorb a large amount of energy and survive the worst case ASSL and environmental operating conditions. A step down transformer can be used to lower the maximum input voltage, but this approach will create problems at low line operation because it reduces the low line input voltage.

The system designer must also consider the effects of voltage spikes. For power supplies that do not have built-in spike suppression circuitry, short-term high-peak power devices, such as metal oxide varistors (MOV), bipolar transient absorbers, or gas discharging tubes, may be used in parallel with the input of the power supply. The size of the device should be decided in accordance with the magnitude and duration of the transient and the amount of energy contained in the transient. EMI filtering may help absorb some of the transient energy, but it should not be considered the only input transient energy absorbing device or circuit for the power supply.

11.1.1.2. Power supply with dc input

Excluding the spike and overvoltage transient, the characteristic of a dc source is basically categorized as Normal Steady State Limit (NSSL), Abnormal Steady State Limit (ASSL) and Emergency Steady State Limit (ESSL). Most commercial-off-the-shelf power supplies do not have a problem operating within the NSSL of the dc power source. Some commercial power supplies may have a problem operating at ESSL and most commercial power supplies will have problem operating at ASSL. When the steady state dc input voltage is higher or lower than the power supply’s input range, a suitable buck or boost dc-dc converter is needed to bridge the gap between the dc input and the supply’s input.

For a spike, the dc input power supply can be protected with a unidirectional or bi-directional device. For cost and size reasons, most commercial power supplies are not designed to withstand and survive the long duration, high Abnormal Steady State voltage, such as the one specified in MIL-STD-704A [B14] or MIL-STD-1275 [B15]. To adapt a commercial dc input power supply to meet the ASSL requirement, the system designer has to add a high energy, long duration transient suppression circuit that is specifically designed to protect against this type of transient. Adding a simple MOV or transient absorber would not be sufficient to handle the long duration, high voltage transient.

The undervoltage transient problem could be resolved by adding more energy hold-up capacitance with a blocking diode between the dc source and the power supply. In some cases, the problem could also be fixed by specifying an oversized power supply.
11.1.1.3. Ac input rectifier and filtering

Many high dc input voltage electronic power subsystems can be adapted to operate with an ac input source by adding an input rectifier and filtering circuit or PFC element. For a power supply with a dc input voltage range of 100V – 200V, adding a full wave bridge rectifier followed by suitable filtering capacitor (electrolytic or other type) will enable it to work with a 115V/60Hz or 400Hz ac input. If the dc power supply’s input voltage range is 200V – 400V, input rectifiers and filtering capacitors should be configured as a voltage doubler so that the dc output voltage is twice the regular full wave rectifier’s output.

An ac to dc conversion stage or isolated PFC element can be used to adapt lower voltage dc input elements such as 48V input telecom converters, to an ac source.

The fundamental ripple frequency on the capacitors with full wave rectification is twice the input line frequency. For the voltage doubler configuration, the fundamental ripple frequency on the capacitors is the input line frequency. The filtering capacitors should be chosen such that the maximum capacitor ripple current is within its rating at specified operating temperature.

Three-phase input is preferred for high power supplies. Benefits of three phase rectification systems include a balanced load on the three-phase ac power source and far less capacitance for the same output voltage ripple as the single-phase rectifier output.

11.1.1.4. Input induced ripple current

For power supplies that are not equipped with an EMI filter or with inadequate filtering, an external EMI filter may be necessary to meet the conducted emissions requirements such as those found in MIL-STD-461E [B10], FCC Part 15 [B12], or DO-160 [B21].

EMI filter selection requires consideration of insertion loss, power handling capability, and maximum voltage rating. In addition, sufficient damping should be provided to avoid an excessively high Q for the filter and to insure stability of the system.

11.1.1.5. Power factor correction

A power factor correction element could be added in front of an ac-input element that does not provide PFC. For a boost-based system the output of a PFC element is normally a dc voltage somewhat higher than the maximum peak of the ac input, and this voltage may not be acceptable as an input to the ac-input element. Before implementing such an adaptation, it is necessary to confirm that it will not adversely affect the performance or reliability of the ac-input element. It is also important that the PFC element can accept the full range of ac input needed in the application.

11.1.1.6. Output voltage and current mismatch

Commonly available output voltages are 1.8V, 2.0V, 2.5V, 3.3V, 5.0V, 12.0V, 15.0V, 24.0V, 28.0V and 48.0V. Most of the electronic power subsystems have an output voltage trimming provision that can be used to adjust the output voltage up or down to meet a particular requirement. For power supplies with multiple outputs, usually only the main output has the trimming provision. Some power supplies have analog or digital output voltage-programming capability.

Some isolated electronic power subsystems can be connected in series to double the output voltage or in parallel (if it is specifically specified in the data sheet) to double the output current if the two electronic power subsystems are compatible. Likewise, two compatible isolated power supplies can be connected in series to provide a positive and a negative output with a common return. The method of using two supplies in series operation is not trouble free. Under certain loading conditions, one of the supplies may have difficulty starting. The failure occurs more frequently when the two supplies are connected with a common return. A possible solution is to add a reverse bias diode across each output.

Two or more electronic power subsystems can be connected in parallel to increase the output current and power if the electronic power subsystems are compatible. To ensure current sharing, select power supplies equipped with current sharing capability.

If the output ripple of the power subsystem is too high, one possible way to reduce ripple is to select power supplies equipped with synchronized operation capability. Adding additional output capacitors can also reduce the peak-to-peak output ripple, but the point of diminishing return will be quickly reached. However, additional capacitors on the output of the power supply may cause the control loop to have stability problems. A more effective, but more costly method is to use additional LC filters at the power supply output. However, this method may not be compatible with outputs using remote sensing. The additional LC filter should not be included within the regulation loop because it may cause the control loop to have severe stability problems.
It is recommended not to connect incompatible power supplies in series or parallel because the operation is unpredictable, including uncontrolled current sharing, output voltage oscillation, or damaged circuits.

11.1.2. Protection
The electronic power subsystem, its electrical source, and its electrical load are susceptible to damage resulting from accidents and faults, such as incorrect electrical connections or damaged internal elements. Protection adaptations can mitigate the damage caused by faults.

11.1.2.1. Input reverse polarity protection
In the event that the input power source is connected in the reverse direction, reverse polarity protection prevents damage to the power supply. Two common approaches to reverse polarity protection are as follows.

11.1.2.1.1. Input series connection
A diode can be placed in series with the input lead so that the reverse current is blocked. The diode requires a voltage rating of at least the maximum expected steady-state voltage, including any transients or surge voltage, plus derating. When the input is connected with the correct polarity, the diode will be forward biased. The diode is required to withstand the maximum input current for steady state operation including any inrush or surge current, plus derating. Additionally, the designer will need to review the thermal aspects of the diode to ensure that the device is properly cooled.

A disadvantage of this approach is the additional power dissipation and its effect on total system efficiency. This is particularly important in higher power systems. Another disadvantage of this approach is the voltage drop of the diode. With low input voltage systems, this can be a large percentage of the input voltage during a low line condition.

11.1.2.1.2. Input parallel connection
Another approach is to place the diode across the input of the power supply in the reversed biased configuration. If the input voltage is connected in the reverse polarity, the diode will be forward biased and will effectively short out the input, causing large amounts of current to flow.

This approach should only be used in conjunction with a series circuit breaker, fuse, or other such devices. The diode will not allow significant reverse voltage to appear across the input of the power supply. A series circuit breaker will trip open due to the overcurrent. The efficiency does not suffer from the effects of the parallel connection as it does in the series connection approach. The diode is required to have a sufficient $I^2t$ rating so that it can survive the event. This is expected to be a one-time thermal event. Regardless, the design should be compatible with the system requirements. Source impedance, sneak paths in the circuit, body diodes in MOSFETs, and delay times should be evaluated.

11.1.2.2. Input undervoltage protection
Undervoltage Protection (UVP) ensures that an element will not be damaged by operation below its minimum rated input voltage. The duration of the undervoltage condition determines how to protect the element. This can be accomplished by monitoring the input voltage and shutting down or removing the input source voltage from the element if the input voltage falls below its rated minimum. There can be situations where a module will be operated at an input voltage lower than specified. It is important to identify the lower limit for the input voltage that will not cause damage to the element and design the shutdown circuit accordingly.

11.1.2.3. Input overvoltage protection
Overvoltage Protection (OVP) prevents operation above an element’s maximum rated input voltage to ensure that it will not be damaged. A line monitor circuit can be used to monitor the input voltage, and activate the OVP circuit in the event of an overvoltage condition. One approach is to operate a series-pass device in front of the element in a saturated mode during normal operation. If the input voltage exceeds the maximum rating, the series-pass device is biased off or in its unsaturated (linear) region, thus allowing the excess voltage to be dropped across the device. For operation in the unsaturated region, the series-pass device can dissipate large amounts of power, therefore this method is usually only practical for transient overvoltage protection. The OVP circuit must react fast enough to prevent damage.
11.1.2.4. **Input transient suppressors**

A transient suppressor is a device that prevents potentially damaging power surges from reaching a power element that is connected to it. Transient suppressors work by collecting and diffusing excess energy, sometimes within a few nanoseconds. The basic function of Transient Voltage Suppressors (TVSs) is to either limit the peak transient voltage through absorption, or divert the energy to another path. A TVS acts as a voltage sensitive switch. Under normal conditions, nothing happens, but when the voltage difference between the power source and the protected line exceeds the threshold, the switch closes and diverts the transient away from the equipment. This switching voltage is often called the "Clamping Voltage" of the TVS. TVSs are available in either unidirectional or bi-directional configurations.

11.1.2.4.1. **Input series connected TVS devices**

When utilizing TVS diodes in series to obtain higher standoff voltages, the sum of the standoff voltages should equal the desired value. One should use devices with the same withstanding voltage rating for series stacking to maximize the total power. If TVSs with different values of withstanding voltage or current rating are used, the device with the lowest peak current capability determines the peak current for the combination of surge protectors.

11.1.2.4.2. **Input parallel-connected TVS devices**

The primary advantage to paralleling TVS elements is increased power and current handling capabilities. However, leakage current will rise in proportion to the number of paralleled TVS devices. The basic requirement is that the devices must be matched for clamping voltage in order to share transient current equally. It is difficult to parallel devices because of circuit parasitics and clamping voltage variations. Careful analysis is important to ensure near equal energy sharing.

11.1.2.5. **Output overvoltage protection**

Overvoltage protection (OVP) adaptation is required when an element does not have intrinsic OVP or its OVP levels are too high to prevent system damage. A monitor circuit can be used to sense the output voltage, and to activate the OVP circuit in the event of an overvoltage condition. Approaches include removing the source power to the element, turning the element off, or crow-barring the output. More than one approach is often used in combination such as crow-barring the output and removing the input power. The OVP circuit must react fast enough to prevent damage. To avoid inadvertent tripping, the circuit must not react too fast, requiring a time delay (a few microseconds) mechanism.

Figure 20 depicts the OV condition sequence of events.
Normal output voltage of the element is shown as $V_0$. At time $t_1$, a fault occurs to cause the element output voltage to start to rise. At time $t_2$, the output voltage reaches $V_1$, the OVP threshold. The OVP condition is sensed but the element is not shut down instantaneously and the output voltage continues to rise. After the OVP delay period $d$, the element is shut down and its voltage falls towards zero.

In order to prevent the output voltage rising as high as $V_3$, an overvoltage clamp can be added, limiting the peak voltage during the time interval $d$ to a value $V_2$. Alternatively, in the absence of a clamping device, one could shorten the delay time to limit the maximum overvoltage level.

11.1.2.6. Output good signal

If an element does not have an “Output Good” signal or if the tolerance does not satisfy the system requirement, then an external voltage window circuit can be added. The circuit is usually composed of two comparators, one for the output voltage rising above the allowable output regulation window, and one for the output voltage falling below the allowable regulation window. The “output good” signal pin will change state should one of these comparators trip. This output good signal can be used in conjunction with additional BIT circuitry to shut down the converter in the event that the output voltage falls outside the designated voltage window. In the case differentiation between overvoltage and undervoltage is required, information for the two conditions is kept separate, but otherwise the two conditions are combined as a single failed condition.

The accuracy of the window detector must be carefully selected with regard to the element’s voltage regulation, refer to Figure 21.
As shown in Figure 21, the element nominal output voltage is $V_{\text{nom}}$, and the specified limits for voltage regulation are between $V_{\text{max}}$ and $V_{\text{min}}$. The upper window detector is set to $V_{UW_{\text{nom}}}$, with tolerance limits between $V_{UW_{\text{max}}}$ and $V_{UW_{\text{min}}}$. It is important to allow a guard band between $V_{\text{max}}$ and $V_{UW_{\text{min}}}$ to avoid incorrect fault detection. In a similar way, the lower window detector $V_{LW}$ also has tolerance and requires a guard band.

11.1.2.7. Output current protection

An element's overcurrent protection is often set at a level higher than is required for safe system operation. In some cases, the element current protection level is externally adjustable. When the desired value of current limiting is not available from the standard stock items, the element vendor may be willing to provide a modified version with a higher or lower current limiting value. The following describe some commonly used output current limiting methods.

11.1.2.7.1. Output hiccup over current limit

Hiccup overcurrent protection circuit monitors the output current level, usually through a shunt (dc) or a current transformer (ac), and removes the output power when the level is exceeded. The hiccup overcurrent protection circuit may remove the output power by commanding an element off. The element remains off for a fixed period of time and is then allowed to restart. If the load fault has been cleared, normal operation will resume, if not the element will shut-down again. The shut down and restart sequence will continue until the load returns to normal levels. Alternatively, a switch controlled by the hiccup overcurrent protection may be used in series with the input or output of the element.

A small delay before activating the hiccup overcurrent protection circuit is often required to accommodate capacitive load turn-on surge currents. The delay time should be long enough that the element will be allowed to reach its normal regulation level. The duty cycle of hiccup circuit should be small enough so that the repetitive surge currents do not damage the element or system circuits. Careful analysis is required to ensure that the element can handle a short circuit but also start up in a maximum load current condition and provide the additional current required to charge the maximum load capacitance. However, if the over load condition is still present during start up, the element needs to be able to shut off again and protect itself or the load from damage.

11.1.2.7.2. Latch off protection

Latch off protection is a scheme that simply shuts the element off in the case of a load fault. The element should remain off until actively told to restart, either by recycling of input power or via a remote enable signal. This type of protection is typically implemented with a current monitor and a comparator to command off the element via its control pin or to control a switch in series with either the input or output of the element.
11.1.2.7.3. Overcurrent fault protection

Overcurrent protection is also required to meet performance and safety guidelines for fault management. This may be as simple as a single input fuse for small subsystems. However, a larger electronic power subsystem will normally contain a number of protection elements (circuit breakers, fuses, etc) for improved protection and fault isolation. The objective is to limit the effect of a failure of one electronic power subsystem element to that portion of the subsystem, allowing the remainder of the subsystem to continue to operate normally. This is particularly important in the case of electronic power subsystems that include redundant elements, since the redundancy is ineffective if the fault is not isolated to a single one of the redundant elements.

Protection elements, particularly fuses, should be sized so that they do not open at maximum current when electronic current limiting is in effect (due, for example, to an external overload or fault outside the electronic power subsystem), but only open in the event of a failure of a particular electronic power subsystem element.

All protection elements must meet the system-level safety requirements imposed by regulatory agencies, such as IEC, UL or CSA, which generally includes specific type approval of the element for use in the appropriate type of application.

11.1.2.7.3.1. Protection element coordination

To achieve the objective of containing the effect of failure discussed above, protection elements (fuses or circuit breakers) must be correctly sized so that under the fault condition the intended element opens and other elements do not open. For fuses, this is referred to as “fuse co-ordination”, and requires that the amount of energy taken to blow the downstream fuse must be within the rated handling energy ($I^2t$) of the upstream fuse. As a rule of thumb, this normally requires that “downstream” fuses are no more than 60% of the rating of the next fuse “upstream”. For circuit breakers a similar consideration applies, but breakers usually have more closely defined characteristics so that less margin is needed. (In this context, upstream refers to fuses near to the source, while downstream refers to fuses nearer the load.)

11.1.2.7.3.2. Interrupt capacity

Each protection element (normally fuses or circuit breakers) must be rated to handle the maximum fault current that could occur in use, by safely opening and extinguishing any arcing before catastrophic damage occurs. The maximum fault current can be determined by considering a direct short-circuit immediately adjacent to the protection element. For example, consider the input circuit breaker in Figure 22 below. The maximum fault current for this element will be the voltage of the source divided by the total resistance in the circuit, including the resistance of the source, the wiring, the connectors, and the circuit breaker. The EMI filter is not part of the resistance in this example, since it is after the breaker.

![Figure 22. Circuit breaker fault current](image)

For subsystems with a low impedance source, the fault current can be very large. In particular, large dc subsystems with battery backup as part of the source can easily have fault currents of many thousands of amps even in circuits with normal operating currents of only a few amps.

11.1.2.7.3.3. Protection element transient

When a protection element opens due to a short circuit in the electronic power subsystem, the source feed inductance and fault current will cause a voltage transient at the source, which will be reflected on all other feeds from that source.
As an example, for telecom systems the voltage waveform in the proposed standard (ANSI T1.315 [2]) is shown in Figure 23. Under a major fault condition, the dc voltage on the 48V input can drop to as low as 5V for about 10ms and then overshoot to 100V before recovering to normal voltage level. (Exact voltages and time intervals vary depending on power system configuration and the magnitude of the fault. The waveform shown represents a realistic worst case.)

Other systems will experience similar transients, although the magnitude and duration will be different for each type of system. System designers should refer to corresponding requirements for details.

![Figure 23. Overvoltage protection response to overvoltage](image)

The standard ANSI T1.315 allows that normal operation of the system may be interrupted during this transient. However, no damage must occur and the system must recover to normal operation following such a fuse-blowing event.

**11.1.2.8. Indicator circuits for ac inputs**

If an ac input “power good” signal is required, there are a number of approaches that can be taken. The best approach will probably be a trade-off of a number of parameters depending on the particular system at hand. In most cases, the circuit that is monitoring the ac line will require isolation between the ac line and the control and monitoring logic. Below are some aspects to consider when using this type of circuit.

For single or three phase inputs, an opto-coupler could be used to monitor the phase-to-phase voltage, or phase to neutral. This will allow the required isolation between the ac circuit and the BIT circuitry. The opto-coupler will need to be a bipolar type otherwise some sort of protection will be required to protect the diode from a possible overvoltage condition on the ac line side. A zener diode could be placed in series to establish a threshold. Another possibility would be an auxiliary winding of an isolation or step down transformer, if one were used in the system. An additional low voltage transformer could be added to provide a scaled and isolated winding. For three phase systems, it is often desirable to determine if one phase has dropped out. This can be done with a delta configuration of opto-couplers.

**11.1.2.9. Indicator circuits for dc inputs**

For dc inputs, an opto-coupler could again be used. This could be used with a simple resistive divider and possibly a zener to establish a threshold trip point for turn on or off. Alternatively, a simple oscillator circuit could be used which is powered by the input bus. This could drive a small signal transformer for isolation to the BIT circuitry. A dc input might not require isolation to the BIT circuitry in which case a non-isolated comparator type circuit could be used.
11.1.3. Stability
The integration of multiple standard elements requires analysis to prove that a system will remain stable. If analysis indicates the potential of instability, the system must be redesigned, and verified at the system-level to be stable within the total operational envelope and environment including all extreme parameters values. Details of the analysis required are beyond the scope of this recommended practice.

11.1.4. EMC
Systems, including the electronic power subsystem, should be analyzed and must be tested, for all mandated EMI/EMC requirements and regulations. The system must pass all EMI/EMC tests, even when individual elements of the system, including electronic power subsystems meet their EMI and EMC requirements. If an electronic power subsystem does not pass the EMC tests, additional filtering, shielding, etc. may have to be added, or else the element performance must be improved as necessary.

11.1.5. Electrostatic discharge
ESD is the rapid transfer of charge (current) between two electrically isolated bodies where a difference in dc voltage is reduced or equalized. This equalization is characterized by fast rise time and short duration. Common sources of ESD include personnel, items made of common plastics, clothing, furniture, processing equipment, and other charged dielectric sources.

The relative motion, physical separation of materials or flow of solids, liquids, or gases generates electrostatic charge. This phenomenon usually occurs in low humidity environments where an object collects an excess amount of charge. ESD may also involve a spark discharge between the capacitively stored charges on one or all bodies involved. After the current flow, the voltage on the mutual bodies is essentially equal. This transfer of electrons, with or without a spark, has been shown to degrade, damage, or destroy electronic circuitry. ESD can damage components by direct contact with a charged source or by charges induced from electrostatic fields in close proximity. Examples of ESD sensitive components are microcircuits, discrete semiconductors, thick and thin film resistors, hybrid devices, and piezoelectric crystals.

All components of a system including the electronic power subsystem must be designed for and protected against ESD effects according to Electrostatic Discharge Control Program such as, MIL-STD-1686 [B8]. At the subsystem-level this can involve careful positioning of elements within the subsystem, and may require additional shielding. At the element level, it also requires consideration of circuit design details and PCB layout.

11.1.6. Isolation and grounding

11.1.6.1. Isolation
In many applications, power subsystems require isolation from input to output, and/or between outputs. In order to achieve the isolation, some (or all) of the elements used in the subsystem design will need to be isolated, with the detailed requirements depending on the configuration of elements used. Electrical isolation is obtained through varying means such as transformer isolation, optical isolation, and or protection device isolation. In most cases the isolation must be built into the elements themselves, and the need for isolation must be considered when selecting elements.

As an adaptation, it may be possible to use non-isolated elements even in a power subsystem which requires isolation, by adding a single isolated element in front of the non-isolated elements.

11.1.6.2. Grounding
There are many issues related to grounding as it affects signal levels, thresholds, noise levels, current loops and EMI/EMC levels, and the details are beyond the scope of this recommended practice. An element might be satisfactory by itself, but when it is integrated into a subsystem, grounding issues may arise. It is the responsibility of the system designer/integrator to ensure that the inclusion of an electronic power subsystem into an over-all system does not introduce any grounding problems. In some cases, grounding requirements may dictate the use of isolated power subsystem elements to allow unrestricted grounding and avoid unwanted ground current loops. Digital, analog, and safety grounds must be connected according to proper engineering practices, and the electronic power subsystem must not violate any grounding requirements.
11.1.7. Electrical terminations
For component level elements, these are typically pins, suitable for directly soldering in CCAs or insertion in connector sockets, or terminals suitable for the soldering of wires.
For card / CCA level elements there is a wider variety of possible terminations, most common being some type of board mounted connector, usually for mating to a motherboard connector in a next higher assembly.
For higher level assemblies such as LRUs these are usually some type of pins, lugs, bus bars, or enclosure mounted connector for mating to a cable assembly in the using system.
Adaptation of electrical terminations is normally a straightforward task, requiring a suitable interconnect assembly with the appropriate connectors for each element and for the system interconnection interface.

11.1.8. Input line
11.1.8.1. EMI
Typically, the user will be concerned with conducted emissions (input noise) on the input lines, conducted EMI interference (output noise) on the output lines, and possibly radiated emissions from the module itself. Conducted emissions on the input (and output) lines are classified into common mode (CM), and differential mode (DM) noise. Common mode noise is typically generated by three sources: switching currents induced into the chassis through components mounted on heatsinks, capacitance between transformer windings, and radiation. Differential noise is generated by the conversion process, primarily caused by discontinuities of the input current waveforms to the main converter transformer.

11.1.9. Output adaptation
11.1.9.1. Output noise
If one or more elements operate on a variable switching frequency technique, the output spikes will vary according to the frequency, and the designer should be aware of this. In certain platforms, particularly sensitive RF equipment, specific frequency bands must remain relatively quiet in order to obtain maximum performance from the equipment. Therefore, the designer must consider the effect of the varying frequency of the noise output when determining the applicability or suitability of specific elements. Usually, elements that use a fixed switching frequency are preferred for low noise applications.

11.1.9.2. EMI/EMC
Almost all products and systems must comply with EMC requirements to meet regulatory limits and to ensure proper operation under all conditions. When designing a power subsystem, it is usually preferable to use elements that include EMI filtering on both input and output, to minimize the propagation of noise currents within the system. However, it is generally not sufficient to use filtered elements, and some additional filtering, is needed to reduce conducted EMI at the subsystem or system level. In many cases, shielding is also needed to reduce the level of radiated EMI. This system level filtering and shielding can also act as adaptation, allowing the use of elements that do not meet system level EMC requirements.
The typical regulatory EMC requirements for various types of products are listed in the following sections.

11.1.9.2.1. Commercial products (USA)
The FCC Rules and Regulations, Title 47, Part 15, Subpart J [B12] regulates "unintentional radio-frequency devices." Products regulated include any unintentional radiator (device or system) that generates and uses timing pulses at a rate in excess of 9kHz and uses digital techniques. This includes most products that have a microprocessor including workstations, personal computers, point-of-sale terminals, printers, modems, and electronic games. To sell or advertise for sale any products regulated under Part 15, Subpart B, their radiated and conducted emissions must have been measured and found to be in compliance. A stand-alone power converter is subject to regulation; also, a system that has an integrated power subsystem is subject to the regulation as a system. Part 15, Subpart B, regulates commercial products. There are two categories; Class A and Class B. Class A uses a verification process and its devices are marketed for use in commercial, industrial or business environments. The Class A limits are listed in Table 7 and Table 8. Class B uses a certification process and its devices are marketed for use at home. Class B limits are more stringent than Class A limits and the Class B certification process is administratively more rigorous than the Class A verification process. The Class B limits are listed in Table 9 and Table 10.
Table 7. Class A radiated emissions (10 meters)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV/m</th>
<th>dB(uV/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 – 88</td>
<td>90</td>
<td>39</td>
</tr>
<tr>
<td>88 – 216</td>
<td>150</td>
<td>43.5</td>
</tr>
<tr>
<td>216 – 960</td>
<td>210</td>
<td>46.5</td>
</tr>
<tr>
<td>&gt;960</td>
<td>300</td>
<td>49.5</td>
</tr>
</tbody>
</table>

Table 8. Class A conducted emissions

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV</th>
<th>dB(uV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.45 - 1.705</td>
<td>1000</td>
<td>60</td>
</tr>
<tr>
<td>1.705 – 30</td>
<td>3000</td>
<td>69.5</td>
</tr>
</tbody>
</table>

Table 9. Class B radiated emissions (3 meters)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV/m</th>
<th>dB(uV/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 – 88</td>
<td>100</td>
<td>40</td>
</tr>
<tr>
<td>88 – 216</td>
<td>150</td>
<td>43.5</td>
</tr>
<tr>
<td>216 – 960</td>
<td>200</td>
<td>46</td>
</tr>
<tr>
<td>&gt;960</td>
<td>500</td>
<td>54</td>
</tr>
</tbody>
</table>

Table 10. Class B conducted emissions

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV</th>
<th>dB(uV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.45 – 30</td>
<td>250</td>
<td>48</td>
</tr>
</tbody>
</table>

The radiated and conducted EMI test procedures are defined in the ANSI Standard C63.4. FCC Rules and Regulations, Part 15 [B12], only regulates radio frequency emissions. Currently there are no FCC regulations for product susceptibility to electromagnetic fields.

Some industries place additional limits on EMI for specific applications. For example, in telecom products connected to analog voice lines there are very strict limits on conducted noise levels in the voice band (300 – 3500 Hz).

11.1.9.2.2. Military products (USA)

EMC requirements for products that are used by the military are contained in a document titled MIL-STD-461 [B10]. This standard can be applied to a wide range of systems including everything from power tools to computer workstations. Unlike the FCC Regulations, MIL-STD-461 includes limits for radiated and conducted susceptibility as well as radiated and conducted emissions. MIL-STD-461 has different limits for conducted and radiated emission as well as for conducted and radiated susceptibility depending on specific application environment and platform. The corresponding test procedures are contained in MIL-STD-462. Table 11, Table 12 and Table 13 below listed the radiated and conducted emission limits for radiated emission (RE102) and conducted emission (CE102) from MIL-STD-461 for Navy mobile and Army ground application with relaxation limits for different voltage.
Table 11. RE102 radiated emissions (ground based)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV/m</th>
<th>dB(uV/m)</th>
</tr>
</thead>
<tbody>
<tr>
<td>2 – 100</td>
<td>15.8</td>
<td>24</td>
</tr>
<tr>
<td>200</td>
<td>31.6</td>
<td>30</td>
</tr>
<tr>
<td>500</td>
<td>79.4</td>
<td>38</td>
</tr>
<tr>
<td>1000</td>
<td>158</td>
<td>44</td>
</tr>
</tbody>
</table>

Table 12. CE102 conducted emission (basic curve, all application)

<table>
<thead>
<tr>
<th>Frequency (MHz)</th>
<th>uV</th>
<th>dB(uV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.01</td>
<td>50119</td>
<td>94</td>
</tr>
<tr>
<td>0.03</td>
<td>17783</td>
<td>85</td>
</tr>
<tr>
<td>0.10</td>
<td>5012</td>
<td>74</td>
</tr>
<tr>
<td>0.50</td>
<td>1000</td>
<td>60</td>
</tr>
<tr>
<td>1.00</td>
<td>1000</td>
<td>60</td>
</tr>
<tr>
<td>10.0</td>
<td>1000</td>
<td>60</td>
</tr>
</tbody>
</table>

Table 13. CE102 limit relaxation for different source input voltage

<table>
<thead>
<tr>
<th>Source Voltage (ac and dc)</th>
<th>Limit Relaxation</th>
</tr>
</thead>
<tbody>
<tr>
<td>28 V</td>
<td>Basic curve</td>
</tr>
<tr>
<td>115 V</td>
<td>6 dB</td>
</tr>
<tr>
<td>220 V</td>
<td>9 dB</td>
</tr>
<tr>
<td>270 V</td>
<td>10 dB</td>
</tr>
<tr>
<td>440 V</td>
<td>12 dB</td>
</tr>
</tbody>
</table>

11.1.9.2.3. Commercial products (non-USA)

EMC requirements vary by country; however, most countries have radiated emissions limits similar to the FCC requirements. Countries in the European Economic Community (EEC) and many other countries have adopted a radiated emissions standard based on a document called CISPR 22 [B13]. CISPR is a committee of the International Electrotechnical Commission (IEC), which provides standards in order to facilitate trade between countries. The CISPR 22 standard categorizes products as Class A or Class B and specifies a test procedure and emission limits that resemble (but are not exactly the same as) the Part 15, Subpart J requirements. Notable differences between the FCC and CISPR requirements are the lower frequency limit for conducted emissions tests and the radiated emission test distances. In addition, CISPR 22 specifies both quasi-peak and average limits for conducted emissions test. FCC limits are all specified as quasi-peak levels.

Again, certain industries may have additional requirements that are stricter than the national standards.

11.1.10. Monitoring and control

11.1.10.1. Monitoring and control of commercial item elements

If monitoring capability is not provided within a subsystem’s elements, monitoring can still be provided by the system controller. For example, output voltage can easily be monitored, output current can be monitored using an external shunt but may affect the regulation. On the other hand, an internal parameter such as a heat sink temperature could not be monitored unless the commercial item is modified.

If a commercial item element does not provide a required control capability, it may also be possible to implement it externally. For example, by adding a series switching element at the input of an element, a remote ON-OFF capability can be implemented. By controlling this element appropriately, in combination with output voltage sensing circuits, the sequencing of output voltage between two or more commercial item elements can be controlled even though the elements themselves do not provide any control capability.
11.1.10.2. Software implementation

In power subsystems where a monitoring and control interface between elements is implemented using a data communication link (such as RS232, or CAN), the software used must be fully taken into account during the system design and integration. This applies at all layers of software and, if they are not fully compatible, one of two actions must be taken:

− Either the differences must be accommodated by an appropriate adaptation function at the power system-level;
− Or else, the design of the data communication link software in the element must be changed.

Because of the large number of possible data communication link software implementations, no attempt is made in this recommended practice to recommend a single solution.

11.2. Mechanical interface adaptation

Table 14 indicates possible mechanical adaptations of elements when there are interface incompatibilities, and indicates what may be the impact in each case. More commonly used adaptations are indicated in bold. More details on each adaptation are described in the paragraphs following the table, as indicated in the column “reference”.

Whenever an adaptation is being considered as a design option, there are several factors that should be fully taken into account, including the following:

− Not all suggestions are practical in all circumstances
− The adaptation may have an impact on performance
− Detailed design and testing is needed to successfully implement the adaptations
− Element designers should be consulted to confirm that proposed solution is appropriate

The total benefits of adapting an existing unit (development cost, unit cost, unit size and weight, time to market, logistics, etc.) should outweigh the cost of alternative implementations.
Table 14. Mechanical interface adaptations

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Element cannot meet</td>
<td>Structural strength, form factor, and resistance to shock and vibration of a</td>
<td>Requires care - may cause damage to element components.</td>
<td>11.2.1</td>
</tr>
<tr>
<td>mechanical requirements</td>
<td>commercial item might be enhanced by use of adhesives or potting.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>for specific product</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>applications</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Element cannot meet</td>
<td>Potting may be used (potting serves two purposes: protection, and insulation)</td>
<td>Increased cost and weight. Potting must be compatible with element</td>
<td>11.2.2</td>
</tr>
<tr>
<td>environmental requirements</td>
<td></td>
<td>design and construction to avoid possible damage</td>
<td></td>
</tr>
<tr>
<td>Inadequate packaging of</td>
<td>Secondary packaging might be required to insert a commercial item into a</td>
<td>Need to ensure element integrity is maintained</td>
<td>11.2.3</td>
</tr>
<tr>
<td>element</td>
<td>subsystem</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Element thermal performance</td>
<td>The following thermal adaptations may be required to fit a commercial item</td>
<td>Requires full analysis and test to confirm performance</td>
<td>11.2.4</td>
</tr>
<tr>
<td>does not meet system needs</td>
<td>into an electronic system: Use of thermal adhesives, heat sinks, heat</td>
<td></td>
<td>11.2.5</td>
</tr>
<tr>
<td></td>
<td>exchangers, heaters and coolers Add a heat shield between the elements and</td>
<td></td>
<td>11.2.6</td>
</tr>
<tr>
<td></td>
<td>the extreme heat Directed cooling fluid may reduce temperature</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shock damping</td>
<td>Shock mounting of electronic subsystems (the use of shock absorbers) may</td>
<td>Common practice</td>
<td>11.2.7</td>
</tr>
<tr>
<td></td>
<td>be used to adapt commercial items for use in high impact environment.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

11.2.1. Structural, structural adhesives, vibration

Structural strength, form factor, and resistance to shock and vibration of a commercial item might be enhanced to meet requirements for specific product applications. These adaptations are common practice in system integration. For cost effective adaptation, it is recommended that the suppliers of original equipment provide clear mechanical specifications.

11.2.2. Potting

Potting serves two purposes: protection, and insulation. Potted modules are usually stronger than unspotted equivalent because potting helps fix components in place. Potting also will insulate components from environmental effects such as humidity, chemical interaction, and in some cases from external heat sources. Potting however might make modules difficult or impossible to test or repair, and unless it is carried out in a very carefully controlled manner it may cause electrical, thermal or mechanical problems. For these reasons, potting is not frequently used for low voltage applications. But it is rather commonly used in high voltage applications where corona or partial discharge is a major concern.

11.2.3. Secondary packaging

Secondary packaging might be required to insert a commercial item into a subsystem. The subsystem needs to be analyzed and tested for the effects of the additional packaging on all interfaces.

11.2.4. Thermal, thermal adhesives, heat sinks, heat exchangers, heaters and coolers

Additional thermal adaptations might be necessary to fit a stand-alone item into an electronic system. These additional thermal adaptations must be based on a thorough thermal and structural design analysis. Alternatives must be considered based on engineering trade-off studies. Selected solutions must be analyzed and tested according to accepted engineering methods.
11.2.5. Extra heat shielding
In some cases, elements designed for certain thermal environments can be adapted for more severe thermal environments by building a heat shield between the elements and the extreme heat. Methods for heat shielding are well developed and are beyond the scope of this recommended practice.

11.2.6. Directing cooling fluid
Subsystems requiring more cooling than can be achieved by conduction might be adapted by increasing the coolant flow to those units. Increasing coolant flow can be accomplished by adding more passages and or increasing the pressure drop across the passage(s).

11.2.7. Shock damping
Shock mounting of electronic subsystems (the use of shock absorbers) is a common practice in adapting commercial items for use in high impact products such as aerospace and automotive applications.

11.3. Environmental interface adaptation
Harsh environments may necessitate that system-level adaptation and accommodation approaches be provided to use commercial item elements or subsystems in environments and systems for which they were not originally marketed. This is done to obtain satisfactory performance and to maintain physical integrity of an element during its specified life. These adaptations may include modifications for extreme temperatures, high humidity, high vibration, long life, or a combination of these environments. Table 15 lists a number of ways different environments can be managed to facilitate the use of commercial items. More details on each adaptation are described in the paragraphs following the table, as indicated in the column “reference”.

Whenever an adaptation is being considered as a design option, there are several factors that should be fully taken into account, including the following:
- Not all suggestions are practical in all circumstances
- The adaptation may have an impact on performance
- Detailed design and testing is needed to successfully implement the adaptations
- Element designers should be consulted to confirm that proposed solution is appropriate

The total benefits of adapting an existing unit (development cost, unit cost, unit size and weight, time to market, logistics, etc.) should outweigh the cost of alternative implementations.
### Table 15. Environmental interface adaptations

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage temperature</td>
<td>Temp screening</td>
<td>Cost of test</td>
<td>11.3.1.1</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Additional cooling/heating</td>
<td>Cost of design and test</td>
<td>11.3.2</td>
</tr>
<tr>
<td>Thermal shock/thermal cycling</td>
<td>Enclosure, encapsulation</td>
<td>Cost, weight</td>
<td>11.3.3</td>
</tr>
<tr>
<td>High humidity and or condensing environments</td>
<td>Coatings</td>
<td>Increased weight</td>
<td>11.3.4</td>
</tr>
<tr>
<td></td>
<td>Environmental seals</td>
<td>Repairability issues</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Drainage channels</td>
<td>Chemical interactions</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Chemical or electrical</td>
<td>Increased power dissipation</td>
<td></td>
</tr>
<tr>
<td></td>
<td>moisture removal</td>
<td></td>
<td></td>
</tr>
<tr>
<td>High impact environments</td>
<td>Vibration isolation and damping</td>
<td>Increased weight and size</td>
<td>11.3.5.1</td>
</tr>
<tr>
<td></td>
<td>Shock isolation and damping</td>
<td>Increased cost</td>
<td></td>
</tr>
<tr>
<td>Corrosive environments</td>
<td>Protective coating</td>
<td>Increased weight</td>
<td>11.3.6</td>
</tr>
<tr>
<td>Chemicals, salt water</td>
<td>Water proofing</td>
<td>Increased cost</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Periodic cleaning</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sand and dust</td>
<td>Sealing</td>
<td>Increased weight and cost</td>
<td>11.3.6.1</td>
</tr>
<tr>
<td></td>
<td>Air filters</td>
<td>Cost of periodic maintenance</td>
<td></td>
</tr>
<tr>
<td>Altitude – Out-gassing/decompression/corona</td>
<td>Encapsulation</td>
<td>Cost, weight, rework, reliability</td>
<td>11.3.6.2</td>
</tr>
<tr>
<td>Explosive atmosphere</td>
<td>Full enclosure</td>
<td>Cost, weight</td>
<td>11.3.7</td>
</tr>
<tr>
<td>Radiated environment</td>
<td>Use of radiation-resistant semiconductors and shielding</td>
<td>Recurring and non-recurring costs</td>
<td>11.3.9</td>
</tr>
</tbody>
</table>

**11.3.1. Storage temperature**

**11.3.1.1. Temperature screening**

Some power product manufacturers design significant margin into their products. This design margin may be taken advantage of when reviewing commercial item hardware for use in harsh environments.

Commercial item manufacturers typically rate their components to operate in temperature environments down to 0°C, -20°C, or -40°C. Testing these items under the expected loading conditions and expected temperature extremes is an effective method of ascertaining whether a component may be satisfactorily used in a particular environment.

A temperature screening plan should be developed that adequately tests component for satisfactory performance for the intended application including margin as defined by the user. Conformal coatings may be used to obtain satisfactory results where temperature changes create condensation.

**11.3.2. Operating temperature**

Adaptation of the local temperature environment, within which an element is recommended to operate, allows the use of the element in extreme system-level environments (where the temperature exceeds the specified temperature range for the item).

In addition to temperature screening, environmental enclosures can be built to insulate an electronic power subsystem module from extreme temperature environments, and to properly heat or cool the device.

Thermal management requires the module to be thermally isolated from the extreme temperature environment. It is important however to have the proper heat sinking or sourcing method to manage heat transfer.

Adding cooling elements to the enclosure may cool a module. For example, cooling may be achieved using gaseous or liquid cooling materials. In some applications, mechanical refrigeration is used to remove the heat from the subsystem to a large radiator. This is commonly used on aircraft.
Cooling, using Thermo-Electrical Coolers (TEC), is an option common in space systems and communications equipment. TEC devices are polarized semiconductor devices capable of transmitting heat in or out of a thermal interface based on the polarity of dc current that passes through the junction between two oppositely charged layers of the material.

For short duration missions, phase change materials may be used to cool a subsystem. Phase change material usually starts as a solid and through the absorption of excess heat, it changes phase to either liquid or vapor.

The use of fans, heat sinks, air fins, and or heat pipes can assist in removing heat from elements as long as the proper heat sinking arrangement is in place.

As an example of a high temperature environment consider electronic power subsystems located near engines in automotive or aerospace applications.

11.3.3. Thermal shock

A commercial item can be physically enclosed, encapsulated, or thermally insulated with suitable materials to effectively protect it from rapid temperature changes that could adversely affect internal electrical and mechanical components.

11.3.4. Humidity with and without condensing environments

Conformal coatings and silicone-based encapsulants are effective means of protecting hardware from high humidity and or condensing environments. The type of coating selected is typically based on the specific requirement, such as access to components/PWB, level of humidity, etc. Listed below are various types of materials, processes, and construction typically used to protect electronics from high humidity/condensing environments.

Parylene - A conformal coating applied to electronic components or assemblies through a vacuum deposition process. The vacuum deposition process used to apply parylene makes it a good choice for assemblies that contain components that are not easily accessible. Parylene is considered to be the most impervious to water of the commonly available coating materials, therefore its’ use is common in 100% condensing environments for more than a 72-hour (typical) continuous period. Parylene provides 240-hours (typical) of moisture protection. Parylene is also used where weight is of extreme concern. Parylene can be removed through an abrasive blasting process.

Acrylic – A conformal coating typically applied through a dip or spray process. Acrylic is a good choice for humid environments that are not 100% condensing for more than a 72-hour (typical) continuous period. Beyond the 72-hour period, absorption of moisture into the protected material is expected. Acrylic is easy to remove for rework using isopropyl alcohol. It should not be used in environment subject to solvent chemical exposure.

Urethane – A conformal coating typically applied through a spray process. Urethane is useful for humid environments that are not 100% condensing for more than a 72-hour (typical) continuous period. Beyond the 72-hour period, absorption of moisture into the protected material is expected. Urethane is easy to remove for rework using isopropyl alcohol.

Silicone compound(s) – A conformal coating typically applied through a spray or dip process. Silicone compound is a good choice for humid environments that are not 100% condensing for more than a 72-hour continuous period. Silicone is easy to remove for rework using mechanical methods. Silicone is less durable than the other materials described above.

Environmental sealing, mechanical means – An effective way to protect hardware from the effects of high humidity, rain, sand and dust, salt atmosphere, chemical or similar environments by fully enclosing the electronics using a material that resists penetration of the expected environmental condition(s). The enclosure design should take into consideration all expected environments. For example, an enclosure used in a salt atmosphere environment would require better sealing due to the corrosive nature of salt atmosphere, than an enclosure used in a less extreme environments.

11.3.5. Vibration and shock environments

There are various methods to adapt and protect commercial item elements to obtain satisfactory results when used in high vibration environments. The methods include, but are not limited to, simple bonding of components to their mating or adjacent structures, partial or full encapsulation, mechanical stiffening structures, mechanical isolation from the next level assembly, etc.

A vibration screening plan should be developed that adequately tests the component for satisfactory performance for the intended application including margin as defined by the user.
11.3.5.1. High impact environment

High impact environment refers to excessive shock, vibration, and or acceleration. In most cases, a combination of all three factors exceeding the normal benign environment prevails.

To mitigate the effects of shock such as in aerospace or automotive applications, shock absorbers may be used. Shock absorbers are designed to dampen or reduce jerk motion caused by sudden shocks so that at the mechanical interface of the element a tolerable shock level is maintained. It is common to mount electronic equipment in aircraft avionics bays or CD players in automobiles on shock absorbing tracks in specifically designed racks. The shock level at the electronics enclosure interface is hence reduced to the levels specified for equipment inside the enclosure.

To reduce the effects of vibration, the subsystem has to dampen continuous motion. This is done by adding friction to the rack mounting. Friction dampens the motion but introduces shear forces that add to the mechanical stress on individual components and whole modules. Fatigue analysis should be conducted to determine the useful life of the subsystem under continuous vibration such as in aircraft avionics or automotive subsystems. Fatigue analysis may be performed using codes such as the CALCE (Computer Aided Life Cycle Engineering) tools developed by a National Science Foundation (NSF) consortium. (See http://www.calce.umd.edu/ for more information.)

High acceleration (positive or negative) may be encountered by aerospace systems, especially during take off and landing; the same is valid to a lesser extent for automotive products. The system at the module level has to be designed and tested to withstand the stress that may be caused by high g levels. Shock absorbing measures include using the proper enclosures on the outside and proper fasteners inside.

11.3.6. Resistance to materials

Many harsh materials exist in special applications from which the commercial item may need protection. These materials include coolants such as Glycol and Coolanol, petroleum products such as oils, gasoline’s, hydraulic fluids, etc. Various materials may be used to encapsulate electronic components or assemblies to prevent contact with the expected environmental materials. Methods available to protect electronics include conformal coatings, full mechanical enclosures, and encapsulants such as epoxy and room-temperature-vulcanizing silicon (RTV). Analysis should be performed to evaluate the suitability of the materials used to encapsulate the electronic components or assemblies.

11.3.6.1. Sand and dust

Contamination from sand and dust environments is typical in industrial and other extreme applications. Commercial items using convection and or forced air cooling should be protected from the effects of sand and dust which include degradation of heat sink mechanisms and degradation, and possible eventual failure, of cooling fans. One method of protecting commercial items from the sand and dust environments would be to use a mechanical enclosure that provides openings for ventilation which include suitable filters to minimize the amount of sand and dust entering the enclosure.

11.3.6.2. Altitude

Commercial items typically do not take into account greater conductor spacing required to operate at high altitudes without degradation or performance failure. Specifically, high voltage circuits must consider possible arcing and corona effects.

11.3.7. Explosive atmosphere

Commercial items may use devices such as un-sealed relays, fuses, fusible links, etc. that may present a hazard if used in an atmosphere where explosive materials exists. Testing should be performed to determine whether the commercial item is usable “as is” or whether additional protection from the explosive atmosphere will need to be provided. Modifications to the commercial item, like parts substitution, may facilitate its use. Alternately, full enclosure of the commercial item may provide adequate protection.

11.3.8. Combined effects

Often two or more of the environments discussed above are encountered. For these cases, multiple adaptations may be required to allow successful use of the commercial item.
11.3.9. Radiation environment

A system exposed to radiation must resist a variety of potentially lethal doses. Exposure to high-energy radiation can result in transient or permanent changes to semiconductor’s material and electrical properties, which can cause electronic power systems malfunction or failure. Designing and producing radiation-hardened electronic power systems requires thorough understanding of the mission (field of use), of the radiation environments, as well as of the system performance and reliability.

Initial decisions for system design are based on whether the field of use will be: (a) commercial (industrial, nuclear power plants, or medical), (b) military (tactical or strategic), or (c) space (commercial or military). In addition, system designers must contend with the applicable radiation environments: (a) total dose ionization, (b) transient dose (dose rate), (c) single event phenomena, (d) neutron radiation, and (e) electromagnetic pulse (EMP). In addition, the system design has to be compliant with the requirements specified in the Radiation Hardness Assurance (RHA) plan to ensure that the radiation hardness capability of the system concurs with the product specifications.

11.3.9.1. Incorporating radiation resistance to total dose ionization

Independent of their field of use, electronic power subsystems are always exposed to the total dose ionization environment. The required radiation resistance at total dose ionization for specific applications is outlined in Table 16. (Table from National Semiconductor Radiation Owner’s Manual, NSC 1999.)

<table>
<thead>
<tr>
<th>Radiation Resistance Level</th>
<th>Application</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 – 3 Krads</td>
<td><strong>Commercial</strong>: industrial, robotic, nuclear power plants, biomedical, space shuttle</td>
</tr>
<tr>
<td>3 – 30 Krads</td>
<td><strong>Tactical</strong>: submarines, tanks, missiles, airborne, ground (field radar, communications)</td>
</tr>
<tr>
<td>20 – 50 Krads</td>
<td><strong>Space</strong>: Space station</td>
</tr>
<tr>
<td>50 – 200 Krads</td>
<td><strong>Space</strong>: Low orbit</td>
</tr>
<tr>
<td>&gt; 200 Krads</td>
<td><strong>Space</strong>: High orbit</td>
</tr>
<tr>
<td></td>
<td>Deep space</td>
</tr>
<tr>
<td></td>
<td>Strategic</td>
</tr>
</tbody>
</table>

Designing and producing radiation-resistance systems is a paramount concern for these applications. Two techniques are employed to achieve this goal: (a) use of radiation-resistant semiconductors, and (b) shielding.

As a preferred alternative, system designers would select semiconductors certified to be resistant to defined radiation levels (RHA). Depending on reliability requirements of the application (specified in the Quality Assurance Plan), rad-hard electronic parts should have the appropriate level of qualification levels and screening flows. For space applications, JAN S parts processed to MIL-M-38510 are frequently selected. For military application the use of parts processed to MIL-STD-883 or JAN B parts processed to MIL-M-38510 is preferred. Also, commercial parts properly uprated or upgraded (screening) can be used. In addition, it is advisable to perform an evaluation of rad-hard semiconductor technologies that will offer full availability by the time the system is in production.

Shielding is necessary for applications lacking radhard parts or parts with insufficient radiation resistance. Local shielding using high-Z materials is frequently used to enhance the semiconductor radiation resistance. Box shielding using Aluminum enclosures is another effective method to increase radiation resistance at system-level.

Determination of the extent of shielding of different types of components depends on the mission [i.e., satellite (commercial or military), tactical (nuclear event), or commercial application (nuclear power plant or medical)].

Because the pound-to-thrust cost ratio of the payload is a critical concern in space applications, better methods, such as radiation-resistant semiconductors, are required to harden a system. Shielding provides little or no protection against the impact of individual galactic cosmic rays (electrons, protons, alpha particles, and heavy ions), energetic neutrons and protons. Where shielding space systems is very expensive, shielding for tactical radiation environments can be economical (notable exceptions are avionics systems, some tank systems, and shipboard equipment). Shielding remains a viable and economical approach for today's industrial, robotic, nuclear power plants, and bio-medical applications.
11.3.9.2. Adaptations for commercial space applications

The commercial radiation environment is comprised of industrial, robotic, nuclear power plants, and biomedical. In addition, space shuttle based electronics is considered to belong to the commercial segment. Land-based commercial applications have the easiest-to-accommodate radiation hardness levels. For these applications, the radiation is generated from the system itself, requiring radiation adaptation of all incorporated electronic subsystems. Major concerns here stem from gamma ray total dose and neutron radiation. Although some equipment parts are exposed to severe hostile radiation environments, most parts can be protected with lead shielding or thick cement walls. In addition, selection of semiconductors with radiation resistant characteristics and use of redundant/fault tolerant power architectures contribute to robust designs. Equipment compliance with EPA, Nuclear Safety Commission, and other safety agencies’ regulations is mandatory.

11.3.9.3. Adaptations for military (USA) space applications

In space environments, the lack of accessibility to institute repairs as well as the space system’s longevity mandate that semiconductors or electronic subassemblies retain complete parametric integrity. Radiation hardness requirements depend on the orbit placement (polar or geosynchronous), orbital inclination, mission duration, and whether semiconductors reside on the satellite's exterior panels or are buried within its body. Radiation-resistant parts with suitable Total Ionizing Dose capability (Krads) are selected. Shielding is mostly limited to equipment enclosure and satellite structure.

The worst space environment is the single event phenomena caused by exposure to galactic cosmic rays and energetic particles. Survivability to this environment is achieved through use of semiconductors with high Linear Energy Transfer (LET) capability (MeV/ cm2/mg). However, there is no semiconductor yet with total immunity to very high-energy particles (> 500 MeV). For this environment redundant architectures (N+1, 2N, N+M) or voting procedures (parallel arrangement of 3 microprocessors) are employed to enhance system’s survivability.

11.3.9.4. Adaptations for military (USA) nuclear hardened applications

Military equipment must address specific detrimental nuclear effects, such as exposure to intense radiation, thermal shock, mechanical shock, and EMP (electromagnetic pulse). Transient (dose rate) radiation and neutron exposure are of major concern in the weapons arena where electronic systems are subjected to very high dose of radiation and neutron fluencies. As a minimum, radhardened military equipment must survive exposure to a nuclear blast, while for critical applications it additionally must be operational.

When designing a tactical system (such as for aircraft, shipboard, ground hardware, or equipment housed in missile silos or ground bunkers), designers must know whether that system must operate throughout a nuclear event, or shut down until the event has passed (just survive).

Survivability of nuclear blasts is achieved by designing in EEE components with proven radiation hardness for high dose rates and neutron fluences. Levels of $10^{12}$ rad/sec for dose rate and $10^{14}$ neutrons/cm² for neutron fluences provide for survivability in most applications. In addition, nuclear circumvention schemes are employed to de-power electronics. A Nuclear Detection Device (NDD) senses the occurrence of the incident radiation caused by a nuclear explosion. Additional control circuitry (operational type) inside of the power supply or end user system is provided to ensure proper sequencing of the circumvention scheme. Upon detection of the nuclear explosion the NDD triggers a sequence of events which: activates crowbar circuits to dump the energy from storage capacitors, inhibits power supply control functions, and imposes a timeout condition longer than the exposure to the incident radiation. Then, the control circuitry commands an orderly restart of the power supplies’ output voltages.

For critical missions, electronics is required to operate throughout the nuclear event. Equipment shielding and rad-hard semiconductors with operation characteristics at survivability levels are required. In addition, for electronic power subsystems, the PWM controller has an imbedded algorithm that provides for a controlled increase of output voltage to make up for the drain of the charge associated with the amount of photocurrents occurring during the irradiation.

EMP environments are addressed at the system-level, not by the semiconductor’s technology. During the nuclear event, equipment is exposed to a strong electromagnetic field with a broad spectrum of frequencies. The fast variation of the electromagnetic field causes unacceptable levels of induced voltages, while some frequency components cause wires to act as antennas. Length of wires is of critical importance, as well as the area of current loops. Rather than risk demise, myriad precautions must be taken to ensure that the power system will survive EMP environments: (a) minimize wires length, (b) use shielded wires and shielded connectors, (c) use connectors with incorporated voltage transient suppressors, (d) use non-inductive routing of the printed wiring boards, (e) use twisted wiring, (f) use voltage transient suppressors on boards, and (g) employ IC’s sockets with incorporated voltage transient suppressors.
11.4. System effectiveness interface adaptation

Adaptations are also possible in the area of system effectiveness, to mitigate the effect of stringent system requirements which may not be met at element level. Table 17 indicates possible system effectiveness adaptations when there are such incompatibilities, and indicates what may be the impact in each case. More commonly used adaptations are *indicated in bold*. More details on each adaptation are described in the paragraphs following the table, as indicated in the column “reference”.

Whenever an adaptation is being considered as an option, there are several factors that should be fully taken into account. The total benefits of adapting an existing element (development cost, unit cost, unit size and weight, time to market, logistics, etc.) should outweigh the cost of alternative implementations.

### Table 17. System effectiveness interface adaptations

<table>
<thead>
<tr>
<th>Interface Incompatibility</th>
<th>Adaptation</th>
<th>Impact</th>
<th>Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reliability and redundancy</td>
<td>Increase MTBF for individual components, design in redundancy</td>
<td>Use of redundancy has major impact on cost, space, and weight</td>
<td>11.4.1</td>
</tr>
<tr>
<td>Vendor qualification</td>
<td>Self-administered procedures such as ISO-9000</td>
<td>Normal practice</td>
<td>11.4.2</td>
</tr>
<tr>
<td>Parts screening</td>
<td>Screen parts</td>
<td>Increased cost</td>
<td>11.4.3</td>
</tr>
<tr>
<td>Product qualification</td>
<td>Pre-planned analyses and tests to insure parts achieve specifications</td>
<td>Normal practice</td>
<td>11.4.4</td>
</tr>
<tr>
<td>Module obsolescence and discontinuance</td>
<td>Last buy, a life-time buy, or redesigning the subsystem with new and or existing replacement parts</td>
<td>Cost of redesign</td>
<td>11.4.5</td>
</tr>
<tr>
<td>Obsolescence management strategies</td>
<td>Many strategies listed</td>
<td>Recurring cost</td>
<td>11.4.5.1</td>
</tr>
<tr>
<td>Availability</td>
<td>Consortia and trade associations can help raise an alarm when sources of components and/or modules are declining</td>
<td>Recurring cost</td>
<td>11.4.6</td>
</tr>
<tr>
<td>Usability</td>
<td>Highlight similarity and mitigate differences</td>
<td>Restricted options</td>
<td>11.4.7</td>
</tr>
<tr>
<td>Installability</td>
<td>Adapt new replacement items</td>
<td>Recurring cost</td>
<td>11.4.8</td>
</tr>
<tr>
<td>Fault tolerance, single point failures</td>
<td>Apply system-level methods to design and test fault tolerance</td>
<td>Improved reliability for subsystem</td>
<td>11.4.9</td>
</tr>
<tr>
<td>Supportability</td>
<td>Logistics and support strategies need to be revised whenever a component and/or subsystem is adapted to use different elements</td>
<td>Cost, availability</td>
<td>11.4.10</td>
</tr>
<tr>
<td>Economic</td>
<td>Specify only to the actual requirements</td>
<td>Excessive specifications increase cost</td>
<td>11.4.11</td>
</tr>
<tr>
<td>Adaptation analysis techniques</td>
<td>Recognizing the value of analysis vs. test</td>
<td>Analysis usually cheaper than test</td>
<td>11.5</td>
</tr>
</tbody>
</table>

#### 11.4.1. Reliability and redundancy

A common measure for reliability is Mean Time Between Failure (MTBF). An accepted method for computing MTBF is MIL-HB-217 (MILL Hand Book 217). Increasing the MTBF for individual components, either by choosing different components or by reducing stress, may increase reliability. Another method used to increase reliability is through redundancy of components, modules, or subsystem. Multiple Module Redundancy (MMR) is a system-level adaptation for increasing reliability and availability of system and is fully described elsewhere.
11.4.2. **Vendor qualification**

Vendor qualification is a means to increase confidence in the ability of a vendor to produce quality products. In the past, Military Qualification was used to insure high reliability. This included MIL-STD-883 for components testing and MIL-STD-38510 for qualifying assembly lines. Recently most military qualification standards have been removed in favor of self-administered procedures. The International Quality Standards, referred to as ISO-9000, are now the most common method for establishing a quality program.

ISO 9000 is concerned with “quality management.” This means what the organization does to enhance customer satisfaction by meeting customer and applicable regulatory requirements and continually to improve its performance in this regard. ISO 14000 is primarily concerned with "environmental management.” This means what the organization does to minimize harmful effects on the environment caused by its activities, and continually to improve its environmental performance; (See [http://www.iso.org](http://www.iso.org).) The purpose of these standards is to establish quality through documented and controlled manufacturing and tests processes.

11.4.3. **Parts screening**

Parts screening is a well accepted method for testing parts to achieve specified levels of reliability. Screening can be expensive and may result in many rejected components or modules.

11.4.4. **Product qualification**

Product qualification is intended to verify that a product meets its interface requirements. Qualification requirements, verified by inspections, analyses, tests and demonstration, are derived from interface requirements and include, but are not limited to, form, fit, function and reliability requirements.

11.4.5. **Module obsolescence and discontinuance**

With the rapid changes in consumer electronic systems, the electronic power subsystems have to keep up with the electronic systems’ capabilities in terms of continuous improvement of all parameters. These include but are not limited to lower output voltage, higher output current, increased efficiency, increased reliability, decreased weight and size, lower unit cost, and ramifications in terms of packaging and component outsourcing (e.g. off-shore manufacturing of components and or modules). Newer and better designs are introduced at a higher rate, displacing older designs that are no longer competitive, making them obsolete. This phenomenon, known as obsolescence, occurs at the technology level and indicates an “unavailability” situation created by the loss, or impending loss of the last acceptable manufacturer of a product. There are several factors contributing to obsolescence:

- Manufacturers introduce new products and obsolete old products to stay competitive
- Corporate mergers causing part/product lines to be consolidated and “redundant” fabrication facilities to be closed
- Component life cycles are shorter than system life cycles
- The technology that defines a part is no longer supported
- Unavailability of a material or an incapability in the supply chain
- New environmental or safety constraints or regulations.

Manufacturers often respond to the aforementioned conditions by discontinuing a specific part or product. Discontinuance is a phenomenon related to a part/product part number level, showing that a manufacturer stops producing it. Discontinuance of electronic power subsystems can be caused by rapidly changing designs to meet cost and performance demands, the high rate of vendor drop out, and a rapidly changing market.

The electronics industry continues to send out notices of plant closure, parts obsolescence, and parts discontinuance. In most cases, users of discontinued components are given a period of time, usually a year, to respond to the discontinuance notice. User options range from ignoring the notice, doing a last buy, a lifetime buy, or redesigning the subsystem with new and or existing replacement parts.

11.4.5.1. **Obsolescence management strategies**

The electronic component obsolescence problem (diminishing manufacturer sources, component unavailability) can sometimes approach crisis proportions for avionics, military, and space industries. For a typical manufacturer of long life systems, greater than 10% of the annual budget is spent on obsolescence, specifically on lifetime buys, carrying costs for components inventory, and designing in alternate components. The effect of obsolescence in military is more profound, because in excess of 18% of the military semiconductors are obsolete components. In addition, military electronics suppliers presently take on support contracts and commitments of typically 25 years.
Frequently obsolete parts are available from aftermarket manufacturers, but at prices of 10 to 15 times the original cost and with serious delivery schedule disruptions (normal turnaround from 4 to 9 months).

Obsolescence forecasting plays an important role in management strategy. While obsolescence is unpredictable by its very nature, there are available means to anticipate procurement problems. Important sources of information are available, as, (a) commercial databases (TACTECH, ITOM, AVCOM, ASPECT), (b) distributors, (c) manufacturer last-time-buy notices, and (d) JEDEC life-cycle coding initiative.

A typical obsolescence management strategy employs three techniques: avoidance, mitigation, and collaboration.

The following are steps that can be employed as avoidance strategies:
- Make component life cycle assessment a formal part of the design review process
- Select components with multiple sources and long life cycle
- Design in components whose next generation shall just plug in
- Re-design before obsolescence actually strikes
- Support open architecture designs that are robust with respect to component changes: also, support modularity to limit the impact of changes
- Utilize programmable logic devices such as fpgas, asics, etc.
- Commit now for design changes to be done in the future
- Institute a judicious procurement plan for production and support parts

Mitigation technique is related to purchasing, operations, maintenance, support, and qualification activities, and is intended to reduce the impact of the obsolescence. The following are steps that can be employed as mitigation strategies:
- Seek alternate sources and last time buy
- Allow replacement components as described in system adaptations in Clause 11.
- Use a data system that provides predictions and rapid notifications
- Adjust equipment approval/qualification processes and work with regulatory agencies to minimize cost impact associated with component changes
- Maintenance plan that includes obsolescence mitigation
- Plan for higher cost replacement components
- Ensure system architectures with low-cost discardable subassemblies
- Reduce systems performance by modifying operations procedures
- Seek local environmental control when wide temperature components cannot be obtained

Collaboration between similar related industries, regulatory agencies, and component manufactures further mitigates obsolescence effects. The following are steps that can be employed as collaboration strategies:
- Aerospace, defense, automotive, telecommunication, medical and other industries to share obsolescence information and consolidate purchases
- Assure that adequate industry standards (IEC, IEEE initiatives) are in place
- Communicate industry need to component manufacturers

11.4.5.2. Specifications

When components become obsolete, the vendors of electronic power subsystems have several choices including:
- Life-time buy to obtain all the components that can continue production for an estimated useful production life;
- Purchase of enough components to extend the life of the electronic power subsystem for another increment of time, several years;
- Embark on an engineering effort to either obtain or develop an equivalent part that will provide a module replacement equal in capability to the product affected;
- Redesign to take advantage of new technologies and in turn issue a discontinuation notice and the introduction of a newer technology substitute. This in turn should allow current users the option of doing life-time buys, or to accept the new design as the replacement after a determined date.
The vendor may also determine that the product is no longer viable and discontinue the subsystem. Issuing a planned end of product life notice with stipulations for similar arrangements as mentioned for vendors of components.

Both vendor and user communities benefit when there is a tracking mechanism for communicating parts obsolescence and parts discontinuation issues. Enough time should be allowed for users to respond either by making life-time buys or design changes.

On rare occasions, the electronics subsystem market experiences a discontinuation of parts and or modules without planned remedies. These situations may be avoided by having an explicit agreement depicting expected action by the vendor and stipulating penalties in case components are discontinued without the proper notification. Figure 24 depicts new products entering the market, reaching a maximum level of usage for a time, and then gradually becoming obsolete. This basic cycle is very short for some essential products, e.g. digital ICs used in supervisory monitoring and controls.

Figure 24. Commercial Item life cycle trends

Capturing legacy and future digital design with VHDL (IEEE-STD-1076) modeling permits easy analysis of future products and reduces cost and risk of development of next generation systems. The same is valid for analog products if accurate modeling is performed using analog and or mixed signal simulations using state-of-the-art tools such as SPICE or VHDL-a (Analog and mixed signal extension of VHDL, IEEE-STD-1076.1).

Configuration management should account for planned system obsolescence and the existence of multiple variations of the same product in the same subsystem or different production runs of the same subsystem. One needs to plan for variations of electronics within a given system, while maintaining functional consistency with equal or improved capability. Improved and/or increased capability should not affect in any way the ability of the new product to satisfy the old requirements.

11.4.6. Availability

Consortia and trade associations can help raise an alarm when sources of components and/or modules are declining. Developing an obsolescence management strategy may allow product continuation by allowing use of developing technologies at a later date, or by mitigating the obsolescence of particular elements.
11.4.7. Usability
Usability is adapting a new product to be placed in use in place of an obsolete component and/or module by
highlighting similarity and mitigating differences.

11.4.8. Installability
Newer replacement items might need to be adapted for one or more of the system interfaces to be able to install and
use in place of obsoleted ones.

11.4.9. Fault tolerance, single point failures
If fault tolerance is not built into an element, system-level methods can be applied to design and test fault tolerance
into updated systems.

11.4.10. Supportability
Logistics and support strategies need to be revised whenever a subsystem is adapted to use different elements. The
revision shall reflect the impact on logistics and support of the replacement technology.

11.4.11. Economic
To produce affordable electronic products, specify only to the actual requirements, because the limits of the
requirements may not be available in combination. System developers should also consider alternatives to
accommodate more cost effective available products. System designers and integrators may need to work with
manufacturer to achieve accommodation and to select the minimum parameter set that satisfies the requirements.

11.5. Adaptation analysis techniques
Recognizing the value of analysis vs. test is important in reducing the cost of adaptation. In many cases the impact
of parameters changes can be assessed using analysis methods rather than through lengthy testing. Examples of
power subsystems analysis tools are SPICE Simulation, VHDL-a Simulation, Radiation Effects Analysis Programs,
and Structure Analysis Programs.
Annex A. (Informative) Bibliography

If the following publications are superseded by an approved revision, the revision shall apply.

[B3] NAVMAT P4855-1A / NAVSO
[B6] ESD-S5
[B17] IEEE Nuclear Radiation Effects Society


Annex B. (Informative) Performance

Parameters have been identified for each of the interfaces described in 4.1. For each parameter, commercially available performance ranges are indicated. The notes column indicates requirements for high reliability or harsh environment applications or other relevant information. This data has been compiled into tables B-1 through B-6. The performance range data is information recorded during the development of this recommended practice that may have changed since its publication.

Operation outside the “Commonly Available” ranges may be possible using adaptations discussed herein. While this recommended practice discusses power elements at a variety of packaging levels, from components through subsystems, performances at packaging levels other than card mountable elements vary too widely to capture the performances that are commonly available. Therefore the table below captures representative, commonly available, performance data for card mountable elements.

B.1. Electrical interface performance
An electrical interface is bounded by the input voltage and the output voltage. There may also be control signals or test points which need to be addressed. There can be various configurations within this boundary whose internal interfaces are unknown. Several elements can be connected together with one element’s output connected to the next element’s input. Elements may be components or cards. Table B-1, Table B-2, and Table B-3 describe electrical performance.

B.2. Mechanical interface performance
The mechanical interface includes size, mounting methods, thermal requirements, external connections, etc. Mechanical performance is shown in Table B-4.

B.3. Environmental interface performance
There are several conditions to consider for environmental performance. The operating and non-operating environments have to be defined. There may be several different environments within one platform such as wing pylons vs. cockpits of fighter aircraft. Performance may also be life expectancy oriented or simply robustness indicators. Table B-5 contains environmental performance.

B.4. System effectiveness performance
System effectiveness performance is concerned with reliability and maintainability. Table B-6 contains system effectiveness performance.
<table>
<thead>
<tr>
<th>Interface Parameter</th>
<th>Commonly Available</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bonding resistance to chassis</td>
<td></td>
<td>Safety Agency Approvals IEC 60950, UL 60950</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td></td>
<td>Vibration, dissimilar metals, current rating, specify</td>
</tr>
<tr>
<td>ESD</td>
<td>Static Sensitive</td>
<td>Handle with ESD precautions</td>
</tr>
<tr>
<td>Isolation:</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input to Output</td>
<td>For isolated elements 50, 100, 500, 1000, 1500, 3750Vdc 500, 1000, 1500, 3750Vdc 500, 1000, 1500, 3750Vdc 50 - 100Vdc</td>
<td>See appropriate regulatory requirements for test methods and conditions Non-isolated converters are available, e.g., PFC, Voltage Regulator Module (VRM)</td>
</tr>
<tr>
<td>Input to Chassis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output to Chassis</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output to Output</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supervisory monitoring and control</td>
<td></td>
<td>Power supply status signals Vendor to characterize: Overload, overvoltage, overtemperature, and, input undervoltage failures. Power on Reset “power good signal” Fan failure, breaker tripped</td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>---------------------------------------------</td>
<td>--------------------</td>
<td>---------------------------------------------------------</td>
</tr>
<tr>
<td>Nominal dc output voltage (Vdc)</td>
<td>1.5, 2.1, 2.5, 2.8, 3.3, 5, +/-5, 8, +/-12, +/-15, 24, 28, 36, 48, 54</td>
<td>Nominal Range 0.8 – 50Vdc (digital &amp; low level analog)</td>
</tr>
<tr>
<td>Regulation, Load (min to full load)</td>
<td>Single or Main output: 0.02% to 1% Static variation about the set point Secondary output: 5% – 10%</td>
<td></td>
</tr>
<tr>
<td>Regulation, Line</td>
<td>Single or Main output: 0.02% - 0.5% Secondary output: 1% –5%</td>
<td></td>
</tr>
<tr>
<td>Regulation, Temperature (drift over rated temperature range)</td>
<td>0.005 – 0.02% / °C</td>
<td></td>
</tr>
<tr>
<td>Regulation, Combined</td>
<td>3%</td>
<td>1% for &lt; 5V 1% - 10% for &gt; 5V which method RSS or extreme value</td>
</tr>
<tr>
<td>Regulation effects due to aging</td>
<td>0.02% / 1000hrs</td>
<td></td>
</tr>
<tr>
<td>Set point voltage accuracy</td>
<td>0.5% to 1%</td>
<td></td>
</tr>
<tr>
<td>Output Voltage Trim Range</td>
<td>-50% to +10% when available (usually single output only)</td>
<td></td>
</tr>
<tr>
<td>Power Density Range</td>
<td>Varies widely based on system architecture</td>
<td></td>
</tr>
<tr>
<td>Voltage Ripple</td>
<td>1% p-p Vout 5V to 50V @ switching frequency 2% p-p Vout &lt;5V @ switching frequency</td>
<td>Specified with a bandwidth limit. May require external filter components to meet its published spec.</td>
</tr>
<tr>
<td>Voltage Spikes</td>
<td>3% p-p Vout 5V to 50V 5% p-p Vout &lt;5V</td>
<td>Specified with a bandwidth limit. May require external filter components to meet it published spec.</td>
</tr>
<tr>
<td>Switching frequency stability</td>
<td>For fixed frequency switching topologies, the operating frequency is typically +/-10% of the initial set point. For variable frequency switching converters, the operating frequency can vary depending on line and load conditions.</td>
<td></td>
</tr>
<tr>
<td>Synchronization</td>
<td>Vendor specifies availability and interface</td>
<td>As required (ref MIL-STD-461)</td>
</tr>
<tr>
<td>Noise spectrum – EMI</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>----------------------------------------</td>
<td>------------------------------------------------------------------------------------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>Voltage programming</td>
<td>Vendor specifies availability and interface</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Analog trim pin</td>
<td></td>
</tr>
<tr>
<td></td>
<td>On/Off control</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Serial interface</td>
<td></td>
</tr>
<tr>
<td>Overvoltage protection</td>
<td>Vendor specifies availability, trip point, and characteristics</td>
<td>Should be sufficient to protect power supply and provide access for shutdown. External circuitry often used to perform this function.</td>
</tr>
<tr>
<td>Undervoltage protection</td>
<td>UV indication may be available</td>
<td>Indication or shutdown usually as a combined fault signal</td>
</tr>
<tr>
<td>Over current characteristics</td>
<td>Straight line</td>
<td>Withstand indefinite overload or short circuit</td>
</tr>
<tr>
<td>Short circuit response</td>
<td>Foldback</td>
<td>Indication may be required.</td>
</tr>
<tr>
<td></td>
<td>Cyclic</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Trip point and tolerance – 104% (defines max operating current) to 125%</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Characterize voltage recovery characteristics</td>
<td></td>
</tr>
<tr>
<td>Hold up time</td>
<td>Vendor needs to specify availability and time</td>
<td>Up to several seconds may be required</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Up to 200ms is common</td>
</tr>
<tr>
<td>Start up trajectory</td>
<td>Vendor needs to provide response characteristic.</td>
<td>Turn on time (20 – 100ms), overshoot</td>
</tr>
<tr>
<td>Power up voltage sequence</td>
<td></td>
<td>Often required for multiple outputs</td>
</tr>
<tr>
<td>Shutdown sequence</td>
<td></td>
<td>Often required for multiple outputs</td>
</tr>
<tr>
<td>Load dynamics</td>
<td>Max di/dt - 0.5A/usec to 30 A/usec</td>
<td>Steploads - Vendor to specify voltage deviation and settling time. Per IEEE Std. 1515-2000</td>
</tr>
<tr>
<td></td>
<td>Steplloads -</td>
<td></td>
</tr>
<tr>
<td>Overtemp Shutdown</td>
<td>Available – characterize when available</td>
<td>Sometimes required</td>
</tr>
<tr>
<td>Overtemp due to short circuit</td>
<td>Characterize voltage recovery characteristics</td>
<td></td>
</tr>
<tr>
<td>Load Impedance Safe Operating Area</td>
<td></td>
<td>Different for each P.S. Design – best approach might be to define a criteria Reactance, max capacitance,</td>
</tr>
<tr>
<td>Output impedance</td>
<td></td>
<td>If a (-) R is present, output impedance needs to be characterized.</td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>----------------------------------------------</td>
<td>----------------------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>Current sharing: Multiple Modules</td>
<td>Sometimes available</td>
<td>Need to know the following:</td>
</tr>
<tr>
<td>Capacity vs. Redundancy</td>
<td></td>
<td>- Current sharing tolerance: 2 – 10%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Current sharing stability characterization</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Response to output short characterization</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Response to control bus failure characterization</td>
</tr>
<tr>
<td></td>
<td></td>
<td>- Capacity vs. redundancy</td>
</tr>
<tr>
<td>Loop stability</td>
<td></td>
<td>$Z_{\text{out}}$, $Z_{\text{load}}$, $Z_{\text{in}}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Gain and phase margin</td>
</tr>
</tbody>
</table>
### Table B-3. Electrical interface source performance

<table>
<thead>
<tr>
<th>Interface Parameter</th>
<th>Commonly Available</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Source Power</td>
<td>48Vdc nom (36 – 75Vdc)</td>
<td>28Vdc, 270Vdc, 115/200 Vac (400 Hz) per (MIL-STD-704, RTCA DO160C,)</td>
</tr>
<tr>
<td></td>
<td>24Vdc nom (18 – 36Vdc)</td>
<td>Backplane voltages 10Vdc, 48Vdc</td>
</tr>
<tr>
<td></td>
<td>300Vdc nom (180 - 375 V dc)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>85V - 264V ac or dc, Universal Input, single phase</td>
<td></td>
</tr>
<tr>
<td></td>
<td>120/240Vac nom (90 – 132 / 180 – 264 V ac, (50 Hz, 60 Hz,))</td>
<td></td>
</tr>
<tr>
<td>EMC (Electro-Magnetic Compatibility)</td>
<td>VDE, UL, CSA, TUV, CE, BABT, FCC</td>
<td>MIL-STDs -461, -462, RTCA-DO160D, VDE, FCC</td>
</tr>
<tr>
<td></td>
<td>Following characterization data is needed:</td>
<td></td>
</tr>
<tr>
<td></td>
<td>EMI:</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Conducted Emissions – 50 kHz to 50 Mhz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Conducted Susceptibility – 30 Hz to 50 kHz</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Radiated Emissions –</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Radiated Susceptibility</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Magnetic fields –</td>
<td></td>
</tr>
<tr>
<td>Power Factor (Harmonic content, loss of 1phase, 3rd harmonic distortion, 3 phase – I/V balance, frequency)</td>
<td>VDE, IEC61000, Power factor correction is not commonly available for 3 phase systems</td>
<td>Boeing requirement, MIL-STD-704, 461</td>
</tr>
<tr>
<td>Inrush Current Profile</td>
<td>Vendor characterization</td>
<td>X times max steady state i^2t limit for &lt; 1ms</td>
</tr>
<tr>
<td>Leakage current to chassis</td>
<td>VDE, UL, CSA, TUV, CE,</td>
<td>MIL-STD-461</td>
</tr>
<tr>
<td>Reflected Ripple Current p-p</td>
<td>&lt;10% of I_m @ switching frequency</td>
<td>MIL-STD-461</td>
</tr>
<tr>
<td>Undervoltage protection (shutdown &amp; recovery characteristics)</td>
<td>ac – ac fail alarm then shutdown</td>
<td>Needs to operate 0 to max V_in with no damage</td>
</tr>
<tr>
<td></td>
<td>dc – Some have undervoltage lockout</td>
<td>Characteristics must define – V_out response from 0 to V_in max.</td>
</tr>
<tr>
<td>Source Impedance as a function of frequency</td>
<td></td>
<td>May be required</td>
</tr>
<tr>
<td>Reverse Polarity Protection</td>
<td>Characterize if available</td>
<td>Sometimes required</td>
</tr>
<tr>
<td>Input Impedance as a function of frequency</td>
<td>Different for each power supply design</td>
<td></td>
</tr>
<tr>
<td>Three phase – phase rotation insensitivity</td>
<td>Vendor characterize if issue</td>
<td></td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>------------------------------</td>
<td>------------------------------------------------------------------------------------</td>
<td>-------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Conduction cooling</td>
<td>Power dissipation at max temp and full load</td>
<td></td>
</tr>
<tr>
<td>Flatness</td>
<td>Thermal I/F flatness – characterization 0.01in/in typical</td>
<td>Total indicator run-out as required</td>
</tr>
<tr>
<td>Maximum base-plate temperature</td>
<td>Characterize maximum operating base-plate temperature (100 °C) at full power</td>
<td>Base-plate temp vs. power curve</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Characterize max operating base-plate temperature at full given power and given environment</td>
</tr>
<tr>
<td>Thermal dissipation area</td>
<td>Characterize in cm² or in²</td>
<td></td>
</tr>
<tr>
<td>Airflow</td>
<td>Airflow – characterization linear feet/min. at STP</td>
<td>Airflow – mass flow rate (at altitude)</td>
</tr>
<tr>
<td></td>
<td>Specify inlet and outlet temperature and flow rate or pressure drop</td>
<td></td>
</tr>
<tr>
<td>Pressure drop/back pressure</td>
<td>Pressure drop – characterize in. of H2O difference between inlet and outlet function of flow rate</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Back press. – characterize source pressure = outlet pressure + pressure loss function of flow rate</td>
<td></td>
</tr>
<tr>
<td>Temp rise</td>
<td>Characterize in °C</td>
<td></td>
</tr>
<tr>
<td>Max Inlet temp</td>
<td>Characterize in °C</td>
<td></td>
</tr>
<tr>
<td>Flow rate – liquid cooling</td>
<td>Characterize in liters/hr</td>
<td></td>
</tr>
<tr>
<td>Pressure drop – liquid cooling</td>
<td>Characterize inches of H2O difference between inlet and outlet</td>
<td></td>
</tr>
<tr>
<td>Pressure drop – liquid cooling</td>
<td>Characterize inches of H2O difference between inlet and outlet</td>
<td></td>
</tr>
<tr>
<td>Cooling medium</td>
<td>Liquid requirement – characterization of: flow rate (liters/hr), type, MSDS, fitting interface, max inlet temperature</td>
<td></td>
</tr>
<tr>
<td>Maximum power dissipation</td>
<td>Maximum expected dissipation for system</td>
<td></td>
</tr>
<tr>
<td>Component Configuration</td>
<td>Provide environment compatible with component requirements such as: cooling, EMI, vibration, and other considerations herein defined.</td>
<td></td>
</tr>
<tr>
<td>Component Mounting</td>
<td>Follow recommendations such as torque requirements, adhesives, soldering etc</td>
<td>Follow recommendations</td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>----------------------------------------</td>
<td>--------------------------------------------------------------------------------------</td>
<td>----------------------------------------------------------------------</td>
</tr>
<tr>
<td>Card/CCA Level Configuration</td>
<td>VME-6U, 3U, SEM(Standard Electronic Mod), Standard Aerospace Module(SAM), PCMCIA, ISA, and others</td>
<td>Define a compatible CCA</td>
</tr>
<tr>
<td>Electrical Connections, component pin outs</td>
<td>Specify location and function Pin/lugs/terminal block, flying leads, connectors Connector keying</td>
<td>User must define a compatible interface Testability access Connector keying</td>
</tr>
<tr>
<td>Durability</td>
<td>NA environmental, sockets not used Specify plating Solderability, corrosion Number of Insertions, Insertion/extraction force</td>
<td>Must comply</td>
</tr>
<tr>
<td>Solderability</td>
<td>Solder temperature and time.</td>
<td>Minimize weight for aircraft, volume (in³, cc)</td>
</tr>
<tr>
<td>Weight/dimensions</td>
<td>Characterize weight (lbs., kg.), overall dimensions</td>
<td></td>
</tr>
<tr>
<td>Package characteristics</td>
<td>Safety certifications such as CE</td>
<td>Flammability UL V94-0 Characterize case material/packaging material- ex. Out-gassing Characterize product marking – durability Characterize case emissivity Hazardous materials statement</td>
</tr>
<tr>
<td>Center of gravity</td>
<td>Not normally available</td>
<td>May be required</td>
</tr>
</tbody>
</table>
Table B-5. Environmental interface performance

<table>
<thead>
<tr>
<th>Interface Parameter</th>
<th>Commonly Available</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>General Note. Make distinction between non-operating and operating</td>
<td>-XX (55) to +XXX (125) °C known aircraft apps, free airflow, worst case environment- pylon, wing, operational/standby, storage higher. (Consider alternatives or relaxation of specification for commercial item applications) RTCA DO-160C, D Basis for operating temperature range defined (qualification test, ATP, etc.)</td>
<td></td>
</tr>
<tr>
<td>Storage temperature range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating temperature range</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Component level</td>
<td>0 to 70 °C – commercial, -40 to 85 °C – industrial (component level) -40 to 100 °C (module level) -20 to 85 °C (assembly level) Specify thermal interface base-plate or ambient temp</td>
<td></td>
</tr>
<tr>
<td>Module level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Assembly level</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal shock/thermal cycling</td>
<td>May be available in different product grades.</td>
<td>Dictated by system design requirements or tailored MIL STDs. Designer to characterize or specify level and method. Define ATP (Acceptance Test Plan) to include ESS (Environmental Stress Screening) and other test procedures as required. Test, analyze, and fix in development and qualification phases. Acceptance test procedures for production.</td>
</tr>
<tr>
<td>Humidity (combined environments)</td>
<td>0 to 95%, non-condensing</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Shock and vibration (could have more impact on power supply systems)</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Designer to characterize or specify level and method. Define ATP (Acceptance Test Plan) to include ESS (Environmental Stress Screening) and other test procedures as required. Test, analyze, and fix in development and qualification phases. Acceptance test procedures for production.</td>
</tr>
<tr>
<td>Resistance to materials (jet fuel, hydraulic fluid, de-icer, gases, corrosive agents)</td>
<td>As required by safety agencies, CE, UL, TUV, VDE, etc.</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Sand and dust</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Fungus</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Salt-spray</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Interface Parameter</td>
<td>Commonly Available</td>
<td>Notes</td>
</tr>
<tr>
<td>-------------------------------------------</td>
<td>--------------------</td>
<td>---------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Altitude – out-gassing/decompression/corona</td>
<td>Up to and including 10,000 feet.</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Explosive atmosphere</td>
<td>As required by safety agencies, CE, UL, TUV, VDE, etc.</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Combined effects (Many Environments @ once)</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Designer to characterize or specify level and method. Define ATP (Acceptance Test Plan) to include ESS (Environmental Stress Screening) and other test procedures as required. Test, analyze, and fix in development and qualification phases. Acceptance test procedures for production</td>
</tr>
<tr>
<td>Acoustic Susceptibility</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Radiation</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Test, analyze, and fix in development and qualification phases.</td>
</tr>
<tr>
<td>Acoustic Emissions/audible noise.</td>
<td>Usually not stated</td>
<td>Dictated by system design requirements or tailored MIL STDs. Designer to characterize or specify level and method. Define ATP (Acceptance Test Plan) to include ESS (Environmental Stress Screening) and other test procedures as required. Test, analyze, and fix in development and qualification phases. Acceptance test procedures for production *May be required for each production unit</td>
</tr>
</tbody>
</table>
## Table B-6. System effectiveness performance

<table>
<thead>
<tr>
<th>Interface Parameter</th>
<th>Commonly Available</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reliability – MTBF</td>
<td>When available, calculated or demonstrated per MIL-STD-217 as requested.</td>
<td>Dictated by system requirements or MIL-STD-217. Physics of failure models.</td>
</tr>
<tr>
<td>Maintainability</td>
<td>Repair or replace</td>
<td>Characterize throw away vs. repair method and repair cost.</td>
</tr>
<tr>
<td>Compliance information, e.g., agency approvals</td>
<td>Identify compliance and agency approvals ex FCC Part 15, BABT, UL, CSA, VDE</td>
<td></td>
</tr>
<tr>
<td>Product life (maintenance items, short life components)</td>
<td>Not available</td>
<td>Awareness of limited life components</td>
</tr>
<tr>
<td>Maintenance Service Interval</td>
<td>Vendor recommendation available</td>
<td>Negotiated</td>
</tr>
<tr>
<td>Derating</td>
<td>Process control methods and certifications disclosed (ISO registration, SPC, screening, ATP)</td>
<td>Process control methods, results, and certifications disclosed</td>
</tr>
<tr>
<td>Quality assurance</td>
<td>&quot;Specifications are subject to change without notice&quot; is typical</td>
<td>Change notification</td>
</tr>
<tr>
<td>Configuration management</td>
<td>'Specifications are subject to change without notice&quot; is typical</td>
<td>Latent defect notification</td>
</tr>
<tr>
<td>Warranties</td>
<td>As stated</td>
<td>As specified per contract requirements</td>
</tr>
<tr>
<td>Test equipment calibration and standards</td>
<td>Per process control</td>
<td>Required</td>
</tr>
<tr>
<td>Product obsolescence</td>
<td>Disclosure when no longer available</td>
<td>Obsolescence mitigation plan</td>
</tr>
<tr>
<td>Qualification process</td>
<td>Per process control</td>
<td>Qualification test report</td>
</tr>
<tr>
<td>Production line final test</td>
<td>Testing process details and data. As specified</td>
<td>Required</td>
</tr>
<tr>
<td>Acceptance testing</td>
<td>Not expected</td>
<td>Required</td>
</tr>
</tbody>
</table>
Annex C. (Informative) Parameter index

This annex indicates the clauses where parameters are discussed. Some parameters applicable at the system-level are defined in IEEE Std. 1515-2000.

Table C-1. General electrical interface parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Where Defined</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bonding resistance to chassis</td>
<td>Per IEEE Std. 1515-2000, 4.9.3 (UUT Grounding)</td>
</tr>
<tr>
<td>Built-in-test</td>
<td>6.3</td>
</tr>
<tr>
<td>Common Mode (CM) interference</td>
<td>6.4.1.2</td>
</tr>
<tr>
<td>Conducted interference</td>
<td>6.4.1</td>
</tr>
<tr>
<td>Conducted susceptibility</td>
<td>6.4.1.3</td>
</tr>
<tr>
<td>Contact resistance</td>
<td>4.3</td>
</tr>
<tr>
<td>Differential Mode (DM) interference</td>
<td>6.4.1.1</td>
</tr>
<tr>
<td>Electrical noise</td>
<td>6.4.3</td>
</tr>
<tr>
<td>Electromagnetic Compatibility (EMC)</td>
<td>6.4, 11.1.4, 11.1.9.2</td>
</tr>
<tr>
<td>Electromagnetic Interference (EMI)</td>
<td>6.4, 10.1.3.4</td>
</tr>
<tr>
<td>ESD</td>
<td>6.4.5</td>
</tr>
<tr>
<td>Grounding</td>
<td>11.1.6.2</td>
</tr>
<tr>
<td>Input overvoltage protection</td>
<td>4.5, 10.2.1, 11.1.2.3</td>
</tr>
<tr>
<td>Isolation</td>
<td>Per IEEE Std. 1515-2000, 4.9.2 (Input- Output Isolation Resistance)</td>
</tr>
<tr>
<td>Lightning</td>
<td>4.11</td>
</tr>
<tr>
<td>Output noise</td>
<td>11.1.9.1</td>
</tr>
<tr>
<td>Overcurrent protection</td>
<td>11.1.2.7</td>
</tr>
<tr>
<td>Power factor correction</td>
<td>11.1.1.5</td>
</tr>
<tr>
<td>Radiated emissions</td>
<td>6.4.2.1</td>
</tr>
<tr>
<td>Radiated interference</td>
<td>6.4.2</td>
</tr>
<tr>
<td>Radiated susceptibility</td>
<td>6.4.2.2</td>
</tr>
<tr>
<td>Remote sensing</td>
<td>10.2.2</td>
</tr>
<tr>
<td>Status monitoring</td>
<td>6.1, 10.4.1</td>
</tr>
<tr>
<td>Supervisory control</td>
<td>6.2</td>
</tr>
</tbody>
</table>
### Table C 2. Electrical output/load interface parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Where Defined</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conducted interference – emissions and susceptibility</td>
<td>Per IEEE Std. 1515-2000, Subclause 4.11.</td>
</tr>
<tr>
<td>Current sharing: multiple modules capacity vs redundancy</td>
<td>Per IEEE Std. 1515-2000, 4.13 (Use of Multiple Power Supplies in a System).</td>
</tr>
<tr>
<td>Hold up time</td>
<td>Per IEEE Std. 1515-2000, 4.6.1 (Hold up Time).</td>
</tr>
<tr>
<td>Input undervoltage protection</td>
<td>4.4</td>
</tr>
<tr>
<td>Load dynamics</td>
<td>Per IEEE Std. 1515-2000, 4.4.7 (Dynamic Load Regulation).</td>
</tr>
<tr>
<td>Load impedance safe operating area</td>
<td>Per IEEE Std. 1515-2000, 3.23 (Load Impedance) and 4.4.2 (Load Voltage Regulation).</td>
</tr>
<tr>
<td>Noise spectrum</td>
<td>6.4.4</td>
</tr>
<tr>
<td>Output impedance</td>
<td>Per IEEE Std. 1515-2000, 4.7.2 (Output Impedance).</td>
</tr>
<tr>
<td>Overtemperature due to short circuit</td>
<td>Per IEEE Std. 1515-2000, 3.29 (Overtemperature Protection) and 4.15.4 (Overcurrent and Short-Circuit Current Protection).</td>
</tr>
<tr>
<td>Overtemperature shutdown</td>
<td>4.6</td>
</tr>
<tr>
<td>Overvoltage Protection</td>
<td>Per IEEE Std. 1515-2000, 4.15.2 (Overvoltage Response).</td>
</tr>
<tr>
<td>Power density</td>
<td>3.2.12</td>
</tr>
<tr>
<td>Power up voltage sequence</td>
<td>Per IEEE Std. 1515-2000, 4.8.1 (Start-up Sequencing/Remote On/Off Control).</td>
</tr>
<tr>
<td>Regulation effects due to aging</td>
<td>4.10</td>
</tr>
<tr>
<td>Regulation, combined</td>
<td>4.9</td>
</tr>
<tr>
<td>Regulation, line</td>
<td>Per IEEE Std. 1515-2000, 4.4.1 (Line Regulation).</td>
</tr>
<tr>
<td>Regulation, load (min to full load)</td>
<td>Per IEEE Std. 1515-2000, 4.4.2 (Load Regulation).</td>
</tr>
<tr>
<td>Regulation, temperature (drift over rated temperature range)</td>
<td>Per IEEE Std. 1515-2000, 4.4.3 (Temperature Regulation).</td>
</tr>
<tr>
<td>Set point voltage accuracy</td>
<td>4.1</td>
</tr>
<tr>
<td>Short circuit response</td>
<td>Per IEEE Std. 1515-2000, 3.38 (Short Circuit) and 4.15.4 (Overcurrent and Short-Circuit Current Protection).</td>
</tr>
<tr>
<td>Shutdown sequence</td>
<td>Per IEEE Std. 1515-2000, 4.8.2 (Turn-Off Sequencing/Remote On/Off Control).</td>
</tr>
<tr>
<td>Start up trajectory</td>
<td>Per IEEE Std. 1515-2000, 4.6.2 (dc Source Inrush Current).</td>
</tr>
<tr>
<td>Synchronization</td>
<td>3.2.14</td>
</tr>
<tr>
<td>Voltage ripple</td>
<td>Per IEEE Std. 1515-2000, 4.5.1 (Output Voltage Ripple).</td>
</tr>
<tr>
<td>Voltage spikes</td>
<td>Per IEEE Std. 1515-2000, 4.5.3 (Switching Spikes) and 3.44 (Transient).</td>
</tr>
</tbody>
</table>
### Table C-3. Electrical source interface parameters

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Where Defined</th>
</tr>
</thead>
<tbody>
<tr>
<td>EMC (Electro-Magnetic Compatibility)</td>
<td>Per IEEE Std. 1515-2000, 3.14 (EMC)</td>
</tr>
<tr>
<td>Input Impedance as a function of frequency</td>
<td>Per IEEE Std. 1515-2000, 4.7.3 (Input Impedance).</td>
</tr>
<tr>
<td>Input voltage spikes</td>
<td>3.2.8</td>
</tr>
<tr>
<td>Input voltage transients</td>
<td>3.2.9</td>
</tr>
<tr>
<td>Power Factor (Harmonic content, loss of 1 phase, 3rd harmonic distortion, 3 phase – I/V balance, frequency)</td>
<td>Per IEEE Std. 1515-2000, 3.33 (Power Factor (Displacement)), 3.34 (Power Factor (Distortion)), 3.35 (Power Factor (True))</td>
</tr>
<tr>
<td>Reflected Ripple Current p-p</td>
<td>Per IEEE Std. 1515-2000, 4.5.4 (Input Induced Ripple Current).</td>
</tr>
<tr>
<td>Reverse voltage protection</td>
<td>4.7</td>
</tr>
<tr>
<td>Sag</td>
<td>4.13</td>
</tr>
<tr>
<td>Source Impedance as a function of frequency</td>
<td>Per IEEE Std. 1515-2000, 4.7.3 (Input Impedance).</td>
</tr>
<tr>
<td>Source Power</td>
<td>Per IEEE Std. 1515-2000, 3.49 (Vnom Input) plus a number of input parameters describing ac and dc source power.</td>
</tr>
<tr>
<td>Surge</td>
<td>4.12</td>
</tr>
<tr>
<td>Three phase – phase rotation insensitivity</td>
<td>Per IEEE Std. 1515-2000, 4.2.6 (Phase Sequence).</td>
</tr>
<tr>
<td>Turn on time</td>
<td>4.8</td>
</tr>
<tr>
<td>Undervoltage protection (shutdown &amp; recovery characteristics)</td>
<td>Per IEEE Std. 1515-2000, 4.15.3 (Output Undervoltage/Overvoltage Indication).</td>
</tr>
<tr>
<td>Parameters</td>
<td>Where Defined</td>
</tr>
<tr>
<td>-----------------------------------------</td>
<td>-------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Airflow</td>
<td>7.3.4.1</td>
</tr>
<tr>
<td>Center of Gravity (CG)</td>
<td>7.2</td>
</tr>
<tr>
<td>Circuit Card Assembly (CCA)</td>
<td>7.1.2</td>
</tr>
<tr>
<td>Component</td>
<td>7.1.1</td>
</tr>
<tr>
<td>Conduction cooling</td>
<td>7.3.1.1</td>
</tr>
<tr>
<td>Convection cooling</td>
<td>7.3.1.1.2</td>
</tr>
<tr>
<td>Cooling medium</td>
<td>3.2.5</td>
</tr>
<tr>
<td>Cooling or thermal energy dissipation process</td>
<td>7.3</td>
</tr>
<tr>
<td>Electrical Connection</td>
<td>Per IEEE Std. 1515-2000 5.4.5 (Connection Types), 5.4.6 (Connection Location)</td>
</tr>
<tr>
<td>Electrical terminations</td>
<td>3.2.6, 11.1.7</td>
</tr>
<tr>
<td>Flow rate</td>
<td>7.3.4</td>
</tr>
<tr>
<td>Forced gas or liquid cooling</td>
<td>7.3.1.1.3</td>
</tr>
<tr>
<td>Heat pipe (phase change)</td>
<td>7.3.5</td>
</tr>
<tr>
<td>Liquid cooling (closed system)</td>
<td>7.3.4.2</td>
</tr>
<tr>
<td>Max inlet temp</td>
<td>7.3.3</td>
</tr>
<tr>
<td>Maximum inlet temperature</td>
<td>7.3.3</td>
</tr>
<tr>
<td>Maximum Power dissipation</td>
<td>4.2</td>
</tr>
<tr>
<td>Mounting</td>
<td>per IEEE Std. 1515-2000 5.4.4 (Mounting Orientation), 5.4.10 (Layout), 5.4.11 (Installation Methods)</td>
</tr>
<tr>
<td>Packaging</td>
<td>7.1, 7.1.3</td>
</tr>
<tr>
<td>Pressure drop/back pressure</td>
<td>7.3.4.3</td>
</tr>
<tr>
<td>Radiation cooling</td>
<td>7.3.1.2</td>
</tr>
<tr>
<td>Solderability</td>
<td>Per IEEE Std. 1515-2000 5.4.11 (Installation Methods)</td>
</tr>
<tr>
<td>Solid physical junction.</td>
<td>7.3.1.1.1</td>
</tr>
<tr>
<td>Temperature rise</td>
<td>7.3.2</td>
</tr>
<tr>
<td>Thermal interface</td>
<td>7.3.1</td>
</tr>
<tr>
<td>Weight/Dimensions</td>
<td>Per IEEE Std. 1515-2000 5.4.3 (Envelope Dimension), 5.4.2</td>
</tr>
<tr>
<td></td>
<td>Footprint</td>
</tr>
<tr>
<td>Parameters</td>
<td>Where Defined</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>-------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>Acoustic Emissions/audible noise.</td>
<td>8.5.2</td>
</tr>
<tr>
<td>Acoustic Susceptibility</td>
<td>8.5.1</td>
</tr>
<tr>
<td>Altitude – out-gassing/decompression/corona</td>
<td>Per IEEE Std. 1515-2000, 5.3.4 (Storage Altitude) and 5.3.7 (Outgassing).</td>
</tr>
<tr>
<td>Combined effects (multiple environments)</td>
<td>3.2.1, 11.3.8</td>
</tr>
<tr>
<td>Dose rate</td>
<td>8.6.2</td>
</tr>
<tr>
<td>Explosive atmosphere</td>
<td>8.4, 11.3.7</td>
</tr>
<tr>
<td>Fungus</td>
<td>Per IEEE Std. 1515-2000, 5.3.14 (Fungus).</td>
</tr>
<tr>
<td>Humidity (combined environments.)</td>
<td>Per IEEE Std. 1515-2000, 5.3.1 (Humidity).</td>
</tr>
<tr>
<td>Neutron radiation</td>
<td>8.6.4</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>Per IEEE Std. 1515-2000, 5.3.9 (Operating Temperature).</td>
</tr>
<tr>
<td>Radiation</td>
<td>8.6</td>
</tr>
<tr>
<td>Resistance to contaminants</td>
<td>8.2, 11.3.6</td>
</tr>
<tr>
<td>Salt-spray</td>
<td>Per IEEE Std. 1515-2000, 5.3.3 (Salt Fog).</td>
</tr>
<tr>
<td>Sand and dust</td>
<td>8.3, 11.3.6.1</td>
</tr>
<tr>
<td>Shock and Vibration (could have more impact on</td>
<td>Per IEEE Std. 1515-2000, 5.3.5 (Mechanical Shock) and 5.3.6 (Vibration).</td>
</tr>
<tr>
<td>power supply systems)</td>
<td></td>
</tr>
<tr>
<td>Single event effects</td>
<td>8.6.3</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>Per IEEE Std. 1515-2000, 5.3.12 (Storage Temperature).</td>
</tr>
<tr>
<td>Thermal</td>
<td>8.1</td>
</tr>
<tr>
<td>Thermal shock/thermal cycling</td>
<td>Per IEEE Std. 1515-2000, 5.3.8 (Thermal Shock) and 5.3.10 (Temperature (Thermal) Cycling).</td>
</tr>
<tr>
<td>Total ionizing dose</td>
<td>8.6.1</td>
</tr>
<tr>
<td>Parameters</td>
<td>Where Defined</td>
</tr>
<tr>
<td>------------------------------------------------</td>
<td>------------------------------------</td>
</tr>
<tr>
<td>Acceptance testing</td>
<td>9.3</td>
</tr>
<tr>
<td>Compliance information</td>
<td>9.4</td>
</tr>
<tr>
<td>Component quality</td>
<td>9.2.2</td>
</tr>
<tr>
<td>Configuration management</td>
<td>9.6</td>
</tr>
<tr>
<td>Derating</td>
<td>9.2.1</td>
</tr>
<tr>
<td>Failure Modes Effects and Criticality Analysis (FMECA)</td>
<td>10.5.1</td>
</tr>
<tr>
<td>Installability</td>
<td>11.4.8</td>
</tr>
<tr>
<td>Logistics</td>
<td>9.5</td>
</tr>
<tr>
<td>Maintainability</td>
<td>Per IEEE Std. 1515-2000, 5.2.1 (Maintainability).</td>
</tr>
<tr>
<td>Part Stress Analysis (PSA) and parts derating</td>
<td>10.5.2</td>
</tr>
<tr>
<td>Parts screening</td>
<td>11.4.3</td>
</tr>
<tr>
<td>Physical product life</td>
<td>9.5.2</td>
</tr>
<tr>
<td>Product discontinuance</td>
<td>9.8</td>
</tr>
<tr>
<td>Product obsolescence</td>
<td>9.7</td>
</tr>
<tr>
<td>Production line certification</td>
<td>9.9</td>
</tr>
<tr>
<td>Qualification requirements</td>
<td>9.1</td>
</tr>
<tr>
<td>Quality Assurance (QA)</td>
<td>9.2</td>
</tr>
<tr>
<td>Reliability – MTBF</td>
<td>Per IEEE Std. 1515-2000, 5.1.3 (MTBF).</td>
</tr>
<tr>
<td>Supportability</td>
<td>11.4.10</td>
</tr>
<tr>
<td>Test equipment calibration and standards</td>
<td>9.3.1</td>
</tr>
<tr>
<td>Usability</td>
<td>11.4.7</td>
</tr>
<tr>
<td>Useful product life</td>
<td>9.5.1</td>
</tr>
<tr>
<td>Vendor qualification</td>
<td>11.4.2</td>
</tr>
<tr>
<td>Warranties</td>
<td>9.10</td>
</tr>
<tr>
<td>Worst Case Analysis (WCA)</td>
<td>10.5.3</td>
</tr>
</tbody>
</table>
Annex D. (Informative) Radiation environments

Radiation is an area that most electronic engineers are not familiar with. Annex D collects some basic knowledge on this topic to assist electronic engineers, system designers and inspectors. Materials presented here are intended to build a working knowledge of the topic.

D.1. Radiation environmental/definition

Radiation is the propagation of energy through space or through materials. The radiated energy is the emission and propagation of waves or particles. Passage of the radiation through matter creates ionization (charge carriers in insulators) or displacement damage (defects in atomic structure). Both radiation effects lead to the performance degradation of the semiconductor device. The following denotes two known types of nuclear radiation environments that can affect electronic systems, and their sources:

- Natural
  - Space and Terrestrial
- Man made
  - Weapons (or nuclear detonation)
  - Nuclear Power Plants
  - Industrial Nuclear Applications

Exposure to high-energy radiation can result in transient or permanent changes to semiconductor’s material and electrical properties, which can cause electronic systems malfunction or failure. In harsh environments, such as space, the lack of accessibility to institute repairs and the space system’s longevity, mandate that semiconductors or electronic subassemblies used in these systems retain complete parametric integrity for long duration missions. Radiation effects are also a concern for tactical and strategic applications, where nuclear weaponry is a threat. Designing and producing radiation-hardened survivable systems is a paramount concern for these applications. Use of radiation-resistant electronic parts and subassemblies is mandatory for radiation sensitive devices in these applications.

D.2. Definition of Terms

D.2.1. Inherent hardness

The level of radiation tolerance exhibited by a product, process, or technology without additional shielding, special processing, or design modifications.

D.2.2. Radiation hardened

This is a device whose inherent hardness has been enhanced or improved through additional shielding, special processing, or through redesign. Radiation hardening may be done either at the component or at the system-level.

D.2.3. Ionizing radiation

Electromagnetic radiation (gamma rays or X-rays) or particle radiation (proton, electron, heavy ions, etc.) having sufficient energy to dislodge electrons from atoms or molecules, are thereby producing charge carriers in its passage through matter.

D.2.4. Burst radiation

Radiation transmitted for short duration at high levels in pulse form. This is also referred to as PROMPT DOSE, PULSE RADIATION (see Dose Rate/Gamma Dot).

D.2.5. Dose rate or gamma dot

This is the amount of ionizing radiation exposure per unit of time normally expressed in rads/sec.
D.2.6. Alpha particles
Alpha particles are helium nuclei, which can easily be stopped with shielding and have negligible effects on electronic devices.

D.2.7. Gamma radiation
Gamma radiation is a highly penetrating electromagnetic disturbance (photons, X-rays, etc) that can emanate from the nucleus of an atom, expressed in units of rads. This type of radiation travels in a waveform much like X-Rays or light, but with a significantly shorter wavelength.

D.2.8. High-energy particle
This is a subatomic particle (heavy ions, protons, etc) with a definite mass and charge moving at extremely high speed and carrying energies of millions of electron volts (MeV).

D.2.9. Annealing (post-irradiation effects)
These are changes in device characteristics that occur after the irradiation of the device has ceased. Annealing may be intentionally induced with a high temperature environment. These effects can cause the device to recover, to partially recover, or to degrade further. These can be short-term or long-term effects.

D.2.10. Total Ionizing Dose (TID)
The amount of the radiation accumulated by the irradiated material during the total time of exposure. TID causes a long-term degradation of semiconductors, which include parametric failures (variations of the voltage thresholds, leakage currents, power consumption, etc) or functional failures. The TID unit is rad (Si), and represents the quantity of any type of ionizing radiation that will impart 100 ergs of energy into one gram of silicon. Gy (Gray) is the standard unit for absorbed dose (total ionizing dose) in the field of radiation dosimetry.

\[ 1 \text{ Gy (Si)} = 1 \text{ J/kg} = 100 \text{ rad (Si)} \]

D.2.11. Displacement Damage
The damage to the bulk structure of a semiconductor device that is caused by the impact of energetic neutrons and/or protons is called displacement damage. Either a nuclear weapon detonation (neutrons) or solar activity (neutrons and protons) can engender this effect. The result of this irradiation is a displacement of the nuclei in a material from their lattice causing device performance degradation or failure.

This is the ionizing radiation response of a semiconductor device caused by the impact of individual galactic cosmic rays (electrons, protons, alpha particles, and heavy ions), energetic neutrons and protons. Responses can include non-destructive effects (single upset, multiple-bit upset, etc) or destructive effects (latchup, gate rupture, burnout).

D.2.13. Single Event Upset (SEU)
A change of state or transient induced by an energetic particle. This occurs in digital components or may have effects in surrounding interface circuitry, a subset known as Single Event Transients (SET). These are “soft” errors in that a reset or rewrite of the devices causes normal behavior to resume thereafter.

D.2.14. Single Event Latch-up (SEL)
SEL is a catastrophic failure that causes an electronic device to generate a low impedance path between two or more voltage sources or a high current density state that results in a loss of device functionality. The latch-up is generated by a parasitic Silicon-Controlled-Rectifier (SCR) structure in an integrated circuit (IC) becoming energized by an ion strike. If permanent damage is not sustained, power cycling of the device is necessary to resume normal operation.

D.2.15. Single Event Burnout (SEB)
SEB is a permanent destruction of a circuit due to a high current state in a transistor. SEB occurs when a high-energy particle hits an off- biased transistor causing a destructive current flow. If the peak current magnitude is large enough, the excessive localized heating condition will result in an electrical short at that site.
D.2.16. Single Event Gate Rupture (SEGR)
A permanent damage of a circuit due to the formation of a conducting path in the MOSFET gate oxide is called a single event gate rupture. SEGR most commonly occurs when an N-Channel mode MOSFET’s $V_{gs}$ is biased negative, and is simultaneously hit by a high-energy particle. Upon impact, the electric field in the gate-drain region collapses leading to a gate rupturing condition in that localized region.

D.2.17. Linear Energy Transfer (LET)
A measure of the energy deposited in material by an energetic particle, in electronic collisions per unit length of its trajectory. The LET unit is MeV/ cm$^2$/mg.

D.2.18. Radiation Hardness Assurance (RHA)
The procedures used to ensure that the radiation hardness capability of a semiconductor device is in compliance with the product specifications.
Radiation hardness assurance categories are shown in Table D-1. Designates guaranteed limits up to a radiation level as stated.

Table D-1. Radiation hardness assurance categories

<table>
<thead>
<tr>
<th>Designation</th>
<th>Radiation Level</th>
<th>Unshielded Environment</th>
</tr>
</thead>
<tbody>
<tr>
<td>M</td>
<td>3 Krad (Si)</td>
<td>Human survival level</td>
</tr>
<tr>
<td>D</td>
<td>10 Krad (Si)</td>
<td>Low-earth orbit; commercial</td>
</tr>
<tr>
<td>P</td>
<td>30 Krad (Si)</td>
<td>Low-earth orbit; military</td>
</tr>
<tr>
<td>L</td>
<td>50 Krad (Si)</td>
<td>Medium-earth orbits</td>
</tr>
<tr>
<td>R</td>
<td>100 Krad (Si)</td>
<td>High-earth orbits or industrial</td>
</tr>
<tr>
<td>F</td>
<td>300 Krad (Si)</td>
<td>High-earth orbits or industrial</td>
</tr>
<tr>
<td>G</td>
<td>500 Krad (Si)</td>
<td>High-earth orbits or industrial</td>
</tr>
<tr>
<td>H</td>
<td>1 Mrad (Si)</td>
<td>High-radiation environment</td>
</tr>
</tbody>
</table>

D.2.19. Radiation Hardness Assured Capability Limit (RHACL)
This is the minimum radiation level that the manufacturer guarantees that a semiconductor device can be exposed to and still meets parametric specifications. It is typically based on data obtained from exposing devices or test structures to radiation in accordance with MIL-STD-883C or MIL-I-38535.

D.2.20. Source Control Drawing (SCD)
SCDs can be used to specify radiation testing to either a Level S or a Level B process flow. SCDs are also used to define tighter radiation-assurance specifications than are available via the RHA’s broader categories.

D.3. Radiation environments

D.3.1. Radiation hardness requirements
Designing and producing radiation-hardened survivable systems requires comprehensive identification of the requirements for system performance, reliability, and mission duration, as well as of the radiation environment. A system exposed to radiation must resist a variety of potentially destructive doses. Initial decisions for system design are based on whether the use will be military or commercial. Radiation hardness requirements also depend on the exposure characteristics and mission duration. When designing a tactical system (such as for aircraft, shipboard, ground hardware, or equipment housed in missile silos or ground bunkers), designers must know whether that system must operate throughout a nuclear event, or shut down until the event has passed. Current radiation hardness needs for applications requiring radiation resistance are generally categorized as outlined in Table D-2.
Table D-2. Application current radiation hardness needs

<table>
<thead>
<tr>
<th>Application Segment</th>
<th>Total Dose</th>
<th>Dose Rate Upset</th>
<th>Dose Rate Latch-up</th>
<th>Neutron</th>
<th>Single Event Upset</th>
<th>Single Event Latch-up</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tactical</td>
<td>&lt;30 Krad(Si)</td>
<td>&lt;10^9 rad(Si)/s</td>
<td>&lt;10^9 rad(Si)/s</td>
<td>&lt;10^13 neutron/cm²</td>
<td>Not applicable</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Avionics</td>
<td>&lt;30 Krad(Si)</td>
<td>&lt;10^7 rad(Si)/s</td>
<td>&lt;10^10 rad(Si)/s</td>
<td>&lt;10^13 neutron/cm²</td>
<td>&lt;1GeV*</td>
<td>&lt;1GeV*</td>
</tr>
<tr>
<td>Space Low Orbit (military)</td>
<td>20-50 Krad(Si)</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>&gt;40 MeV/(mg/cm²)</td>
<td>&gt;100 MeV/(mg/cm²)</td>
</tr>
<tr>
<td>Space High Orbit (military)</td>
<td>100 Krad(Si) – 1 Mrad(Si)</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>Application dependent</td>
<td>&gt;40 MeV/(mg/cm²)</td>
<td>&gt;100 MeV/(mg/cm²)</td>
</tr>
<tr>
<td>Commercial Satellites</td>
<td>20 – 100 Krad(Si)</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>&gt;40 MeV/(mg/cm²)</td>
<td>&gt;100 MeV/(mg/cm²)</td>
</tr>
<tr>
<td>Strategic systems (military)</td>
<td>&lt;1 Mrad(Si)</td>
<td>&lt;10^12 rad(Si)/s</td>
<td>&lt;10^14 rad(Si)/s</td>
<td>&lt;10^14 neutron/cm²</td>
<td>&gt;40 MeV/(mg/cm²)</td>
<td>&gt;100 MeV/(mg/cm²)</td>
</tr>
<tr>
<td>Nuclear (power plant)</td>
<td>LOCA**</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>Not applicable</td>
<td>Not applicable</td>
</tr>
<tr>
<td>Robotics &amp; Biomedical</td>
<td>Unknown</td>
<td>Unknown</td>
<td>Unknown</td>
<td>Unknown</td>
<td>Unknown</td>
<td>Unknown</td>
</tr>
</tbody>
</table>

* Single event upsets or single event latch-up may occur when radiation impacts ICs at atmospheric altitudes
** LOCA: Loss of Coolant Accident

Note: Table from National Semiconductor Radiation Owner’s Manual, NSC 1999.

In the past, radiation-sensitive space systems have been shielded using a variety of shielding materials. However, because the pound-to-thrust cost ratio of the payload is a critical concern, better methods, such as radiation-resistant semiconductors, are required to harden a system. Whereas shielding space systems is very expensive, shielding for underground tactical radiation environments and stationary industrial systems can be economical. Shielding is not used for most tactical systems. One exception is tanks. Shielding remains a viable and economical approach for today's industrial, robotic, nuclear, and bio-medical applications.

D.3.2. Major radiation environments

Four major radiation environments can cause concern with respect to the use of semiconductors: total ionizing dose, transient radiation (dose rate), single event phenomena, and neutron radiation. A semiconductor manufacturer can minimize these effects through layout, design rules, manufacturing process design, and circuit design. The fifth major environment, the electromagnetic pulse (EMP) is relegated to system designers and manufacturers of total systems and is addressed as part of the system design criteria.

D.3.2.1. Total ionizing dose

The total dose environment can include a composite of gamma rays, X-ray radiation, and other ionization radiation. The total amount of absorbed radiation energy varies according to the absorption material. Parametric concerns include changes to stand-by current, leakage currents, threshold voltages, and propagation time delays.

D.3.2.2. Transient (dose rate) radiation

Transient irradiation is associated with nuclear explosion and is a major concern for designers of strategic equipment. Characterized by a narrow pulse width (usually between 3ns to 10µs) containing a total dose of 1000 rad (Si) or greater, it represents the amount of total dose irradiation given in a specified time interval. A dose rate pulse will generate excess charge in a short period of time. Adverse effects of transient irradiation include upset (soft error), latch-up, junction burn-out, short transient pulse on the output, and saturated outputs, which depend on the amount of photo-current (excess charge) generated and the output loading.

D.3.2.3. Single event phenomena

Charged particles or neutrons can induce single event phenomena:
− Heavy ions from solar flares or galactic cosmic rays can initiate SEE in transistors. Outside of the Van Allen Proton Belts, heavy ions normally provide the worst-case single event effects (SEE) environment for electronic space systems.
− Alpha particles are the result of the decay of radioactive materials and cause single event effects. Thorium, a radioactive material used in ceramic packages, is a source for alpha particles. Packaging materials and solder containing radioactive isotopes are primary source due to their close proximity to semiconductor device.
− High-energy protons in the Van Allen Belts, or protons injected by solar flares, can cause single event effects. Protons having energy greater than 10MeV may induce an SEE.
− Neutrons, similar to high-energy protons, can interact with semiconductor lattice atoms thus producing charged particles to induce ionization. High-altitude environments 50,000 to 80,000 ft above sea level can be a large source of neutrons.

Detrimental single event effects on electronic systems include transients, soft error, and permanent damage. Exposure to this environment can cause catastrophic failure in power MOSFETs in two ways: (a) single event gate rupture, and (b) single event burn-out. In general terms, if a semiconductor device does not suffer from single event upset or latch-up in a heavy ion environment, it should not be affected in a high-energy proton or low-energy alpha environment.

D.3.2.4. Neutron radiation

Neutron radiation-induced defects significantly affect the electrical behavior of semiconductor devices. In bipolar devices, it causes lattice structure damage; thereby affecting a device's minority carrier lifetime and transistor gain. CMOS technology is immune to neutron irradiation below \(10^{14}\) neutrons/cm\(^2\). The effect of neutron radiation on power MOSFETs is negligible for most applications, however at fluencies exceeding \(10^{12}\) neutrons/cm\(^2\), the effect must be taken into consideration especially in systems containing bipolar devices (TTL, ECL, I\(^2\)L, etc.). Note that high fluencies of protons can produce similar effects (see Subclause D.3.3.1).

D.3.3. Radiation damage effects
Two types of radiation damage effects occur in solid-state (semiconductor) electronic products: displacement damage and ionization effects.

D.3.3.1. Displacement damage
Displacement damage within the semiconductor material results from high-energy particles (protons or neutrons) causing crystal lattice defects. These defects are known as vacancies, di-vacancies, interstitials, or defect clusters. These defects generate energy levels in the forbidden band-gap of the semiconductor. These defects affect lifetimes and carrier mobility, which cause degradation or possible failure of the integrated circuit. Bipolar products are most susceptible to displacement damage due to the importance of carrier lifetimes in the transistor base region. Silicon based materials are more susceptible to displacement damage than 3-5 compounds such as Gallium-Arsenide (Ga-As).

D.3.3.2. Ionization effects
Ionization damage effect is the generation of electron-hole pairs within the material when charged particles penetrate the semiconductor or oxide material. The resulting effects of this ionization are the generation of photocurrents or trapped charge in oxides. These ionization damage effects are responsible for parasitic leakage paths and threshold voltage shifts.

D.3.4. Space and military environments
Most of the radiation-hardened electronic systems are designed and produced for military and space applications.

D.3.4.1. Space environment
The natural space environment contains four main sources of radiation: protons and electrons trapped in the Van Allen Belts, heavy ions trapped in the magnetosphere, cosmic ray protons and heavy ions, and protons and heavy ions from solar flares. The level of all sources is affected by the activity phase of the sun (minimum or maximum), while radiation effects are mission-dependent based upon the satellite orbit altitude, inclination, and trajectory. The predominant radiation effects for the natural space environment are the total ionizing dose and the single event effects.
D.3.4.2. Military environment

The military environment is generally equated with the nuclear explosion event. In a nuclear explosion at the Earth's surface, there is a high dose rate gamma flux (typically $>10^8$ rads (Si)/sec), a delayed total ionizing dose less than $10^4$ rad (Si), and a neutron fluence (greater than $10^{14}$ neutrons/cm$^2$). The X-rays generated at the Earth's surface are absorbed by the surrounding air and are responsible for the large nuclear fireball. In contrast, these X-rays are not absorbed in space and travel very long distances outside the atmosphere. The predominant radiation effects for the military applications are displacement damage, transient dose rate, and total ionizing dose. Additionally, military equipment must address other detrimental nuclear effects, such as thermal shock, mechanical shock, and EMP (electromagnetic pulse). Current radiation concerns for military applications requiring radiation resistance are generally categorized as outlined in Table D-3.

Table D-3. Types and sources of radiation for military applications

<table>
<thead>
<tr>
<th>Environment</th>
<th>Radiation Source</th>
<th>Strategic</th>
<th>Space</th>
<th>Tactical</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrons, Protons, Cosmic Rays, etc.</td>
<td>Space environment</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>β-Particles</td>
<td>Electrons emitted by fission fragment</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>X-Rays</td>
<td>Blackbody Radiation</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Neutrons</td>
<td>Radiation emitted during the fission and fusion processes</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Prompt Gamma Rays</td>
<td>Radiation emitted during the fission and fusion processes</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>Delayed Gamma Rays</td>
<td>Fission fragment radiation</td>
<td>X</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Electromagnetic Pulse (EMP)</td>
<td>Generated by electrons stripped from air atoms by prompt gamma rays</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>System Generated EMP</td>
<td>Radiation bombardment of metallic bodies</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Thermal</td>
<td>Thermal energy radiated by fireball</td>
<td>X</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Blast</td>
<td>Shockwave generated in air by explosion</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
</tbody>
</table>

Note: Table from “System Survivability in the Nuclear Age,” Defense Science & Electronics, July 1985

D.4. Radiation design considerations

Designing a radiation-hardened system requires a thorough understanding of the system's mission relative to its potential radiation environments, and the equipment environmental requirements. The following steps are commonly used to ensure the best RHA (Radiation Hardness Assurance) design methodology:

D.4.1. Conceptual design

When designing a radiation-hardened system, guidelines must be based on the system's mission and required survivability. Experience has shown that the most effective means of reducing uncertainty factors and design margins in particle predictions is to define for the mission: (a) when the mission will start, (b) where the mission will occur, (c) what is the mission duration, (d) when the systems will be deployed, (e) what subsystems must operate during worst case environment conditions, (f) what subsystems are critical to mission success, and (g) the amount of shielding surrounding the radiation-sensitive parts.
D.4.2. Engineering development phase

During this phase, design activities shall comply with the program development Radiation Hardness Assurance Plan (RHAP) requirements. To ensure the best Radiation Hardness Assured design, it is necessary to understand the complete radiation response of each component in the system, e.g., what electrical parameters are affected by which radiation environments. This includes variable and functionality (attribute) data to the level of radiation failure. Variable data as performed in a step-stress radiation approach permits observance of non-monotonic behavior for each electrical parameter's radiation response. In addition, a Radiation Analysis may be required to understand the combined effect of the parametric degradation of components.

Usually the RHAP: (a) defines the assumptions and models used to calculate the incident radiation environment, (b) discusses methods to calculate the internal ionizing and the non ionizing radiation environment, and the resulting effects, (c) provides EEE parts test and analysis guidelines to ensure completeness and consistency in reporting and analyzing EEE part radiation response and qualification, and (d) provides system-level verification reporting requirements that will allow equipment total dose, dose rate, displacement damage and SEE rates to be folded into higher level reliability calculations.

D.4.2.1. Incident radiation environment

The radiation environment specifically applicable to the mission must be defined before commencing radiation design. Two components of the radiation environment must be provided:

- Mission dose depth curve for the electrons and protons environment over the orbital design life indicating the total dose attenuation versus shielding material thickness.
- Linear energy transfer integral spectra for galactic cosmic ray and anomalous large solar flare conditions used to compute single effect phenomena occurrence probability and effects.
- Dose rate and neutron fluence levels occurring during nuclear events.

D.4.2.2. Radiation evaluation process

With a fully defined radiation environment for the mission, a radiation evaluation of the parts hardness is possible. A radiation evaluation process flow is shown in Figure D-1.

- Sector analysis at system and equipment level is used to determine the radiation exposure (dose levels) for all radiation sensitive parts inside of the equipment. This analysis employs the proposed (a) structural model of the spacecraft/vehicle, (b) equipment position, and (c) equipment structural model. Total dose levels to be received at component (die) level are calculated taking into account spacecraft/vehicle shielding. Total dose simulations can be performed either using 3D sector based codes or 3D Monte Carlo transport codes.
- Parts radiation hardness analysis is conducted based on the Declared Parts List and radiation databases (US-JPL, US-NRL, ESA, and others). Each EEE part is characterized with respect to total dose tolerance, displacement tolerance, and single event effects error rate prediction. An EEE part earns radiation validation for the application if it meets all requirements specified in the RHAP. In most cases a part would be automatically validated if all the following requirements are met:
  - The part TID capability is higher than the dose exposure level specified in the RHAP (including the safety margin)
  - The part LET capability for SEE is higher than the dose exposure level specified in the RHAP (including the safety margin)
  - The part survivability dose rate and neutron fluence levels are higher than the RHAP specified values
  - Radiation database test data indicates that radiation testing was perform in accordance with MIL-STD-883E, MIL-STD-750C or ASTM (American Society for Testing and Materials) test methods and procedures
  - Test biasing conditions were worse or equivalent to the application conditions.
If the part radiation capability is lower than the specified design margins, the part is considered a radiation sensitive part. For radiation sensitive parts, lot testing may be required if design margin requirements are not met. In addition, radiation sensitive parts may be validated if suitable risk reduction measures, such as additional shielding, are implemented.

Radiation worst-case analysis is performed using previously calculated parts sensitivity and radiation levels for the equipment. The final objective is to determine equipment and spacecraft/vehicle worst-case performance over the length of mission, taking into account radiation effects, aging and other causes of part(s) degradation. Single Event Effects rates on sensitive parts will be quantitatively calculated for implementation in the worst-case analysis. Total ionizing dose and displacement induced drifts are extrapolated from test reports for implementation in the worst-case analysis. EEE parts can be validated for use depending on their ability to withstand the relevant radiation environment. Not-validated EEE parts may be used if suitable risk reduction measures can be implemented.

- Risk Reduction Actions are used to validate the use of radiation sensitive EEE parts:
  - Assessment of EEE critical parts using highly accurate simulation of dose levels received at die level and SEE error rate prediction
• Radiation testing at low dose rates of the application critical linear bipolar devices to fully characterize the Enhanced Low Dose Rate (ELDR) effects
• Radiation testing of flight lot parts during procurement for EEE parts with insufficient design margin,
• System and equipment level countermeasures to increase acceptability of the radiation sensitive parts through additional shielding at component level (spot shielding) or at box level (additional thickness of box cover), use of redundant components or functions, use of Nuclear Detection Devices (NDD) to turn off power during exposure to the incident radiation coming from nuclear events, implementation of error correction algorithms, specific memory organization, latch-up protection, and suitable derating to prevent SEB/SEGR.

D.5. Radiation testing

D.5.1. Radiation-effects testing
Radiation testing is mandatory for radiation-sensitive EEE parts and systems associated with the following applications: (a) satellite and avionics, (b) military strategic and tactical, and (c) nuclear power plants, and (d) therapeutic radiation sources. Each of these applications has unique semiconductor-device radiation-hardness testing requirements. Because radiation effects result from many different physical phenomena, each radiation environment demands its own test techniques and procedures for measuring its effects on electronic devices. Furthermore, ensuring that an electronic system achieves specified radiation-hardness requires an array of tests incorporating different test methods.

D.5.2. Executing radiation-effects testing
Radiation affects testing complexity and high cost demand detailed planning and preparation. Four important elements in radiation test planning are (a) Radiation Test Plan, (b) Radiation Test Procedure, (c) Radiation Dosimetry, and (d) suitable Radiation Facilities.

The Radiation test plan covers all of the system’s test requirements and defines the process for carrying out a particular test procedure. It includes test-sample(s) selection, personnel, organization and responsibilities, facilities, and measurement and calibration equipment. It also includes a step-by-step description of the test (each function performed requires a separate description that includes the timing of post-radiation measurements), documentation (which includes sign-off forms, data format and identification of test conditions with data), and final data processing and analysis.

Individual Radiation test procedures are developed from the radiation test plan. A radiation test procedure describes test requirements for a single device or electronic system type. A radiation test procedure defines major areas including part number, package type, and number of leads and pin-outs, serial number, lot and wafer numbers of devices to be irradiated. It also defines operating conditions during radiation exposure, total dose and dose rate for each exposure, device pre-radiation parametric values and test conditions, bias-circuit diagrams showing locations of all circuit elements during each measurement; whether the test is to occur in-flux (during irradiation), required device parameter measurements, and operating conditions during those measurements. In addition, it contains a list of all test fixtures and test equipment for the test, and a description of test-data formats, and information on radiation facility.

Radiation dosimetry is extremely important. The use of incorrect dosimetry can invalidate all test results. The most common dosimetry system for total dose measurement is the Thermo-Luminescent Dosimetry (TLD). TLD uses hot pressed polycrystalline Lithium Fluoride (LiF) chips that absorb a portion of the radiation energy in the form of electrons that remain trapped in the LiF lattice for a very long time at room temperature. Once heated to about 150°C, the lattice releases this electron energy as light. A cooled photo-multiplier measures thermo-luminescence, integrating the signal emitted over a particular swept temperature range. The integrated charge from the tube is roughly proportional to radiation exposure over several orders of magnitude and thus, with calibration, the charge indicates dose received. The American Society for Testing and Materials (ASTM) approved a standard for TLD use in radiation testing, ANSI/ASTM E668-78. This standard specifies procedures using the TLD dosimetry to calibrate gamma-radiation fluence within 10% accuracy at each position from the source, and the calibration must be traceable to the National Bureau of Standards. Dosimetry at each location should be uniform to within 15% for most applications. For Cobalt-60 sources, once the field is calibrated, if the exposure geometry remains fixed, only test validation by a specific test procedure requires further dosimetry. Because of source half-life, decay must be calculated and applied at least every two months for determining dose rate.
Electron and proton accelerators require measuring radiation fluence for each exposure. For charged particle beams, a metal block of appropriate thickness can stop all particles while allowing measurement of particle flow to ground. This arrangement is known as a Faraday cup, and refined forms control most electron and proton machines. The main refinements are evacuation of air around the cup electrode and shaping it as a long thin cavity so that secondary electrons do not escape. Presetting the desired fluence limits on an integrating controller eliminates errors that may arise from beam-current fluctuations.

Choice of the correct Radiation facility, one of the most important considerations for total-dose-radiation testing, depends on device types under test. Devices that are sensitive primarily to ionization damage require testing using either a Cobalt-60 gamma source or a steady-state dc electron accelerator. Devices that are sensitive primarily to displacement damage require a steady-state dc electron accelerator or a proton accelerator, producing a flux of electrons or protons with sufficient energy to penetrate the shielding material and enter the sensitive electronics underneath.

D.5.2.1. Radiations sources and test methods for total dose testing
Radiation sources for total-dose testing include X-rays, Gamma rays (Cobalt-60, Strontium-90, Cesium-137), electrons and protons. Each type of source affects the device under test differently, depending on the source’s energy. Each environment also exhibits a specific energy spectrum. Therefore, the correct source and energy for each application must be identified. The most common source for radiation testing is Cobalt-60. For military systems, a total-dose radiation test plan should follow MIL-STD-883E Test methods 1019.4 and 1019.5 requirements.

D.5.2.2. Radiations sources and test methods for neutron testing
Neutron irradiation source is a nuclear reactor. Neutron testing normally requires reactor calibration to a 1-MeV equivalent spectrum. MIL-STD-883E Test method 1017 specifies neutron damage test requirements for military systems.

D.5.2.3. Radiations sources and test methods for dose rate testing
Dose-rate testing normally employs a pulsed linear accelerator (LINAC) or Flash X-ray machine. MIL-STD-883E Test methods 1020 and 1021 outline military dose-rate test requirements.

D.5.2.4. Radiations sources and test methods for SEE testing
SEE testing is conducted with heavy ions or protons. The device under test is placed in the beam line of a cyclotron or particle accelerator. Military standard test methods for SEE testing have not been developed, so there is no MIL-STD yet. However, heavy ion testing can be conducted according to the ASTM Test method F-1192M-95.