High Density Integrated POL Converters

Presented by

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The Bradley Department of Electrical and Computer Engineering
Virginia Tech

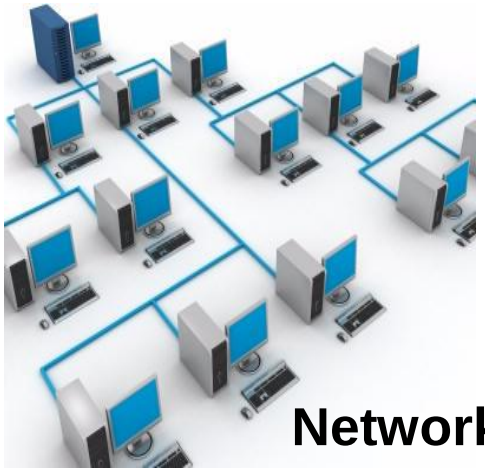
POLs in Computer and Telecom Industries

Telecom

Server

Laptop

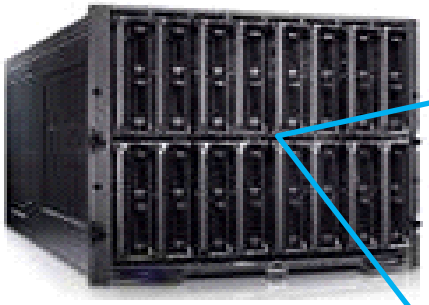
POL for IT Industries



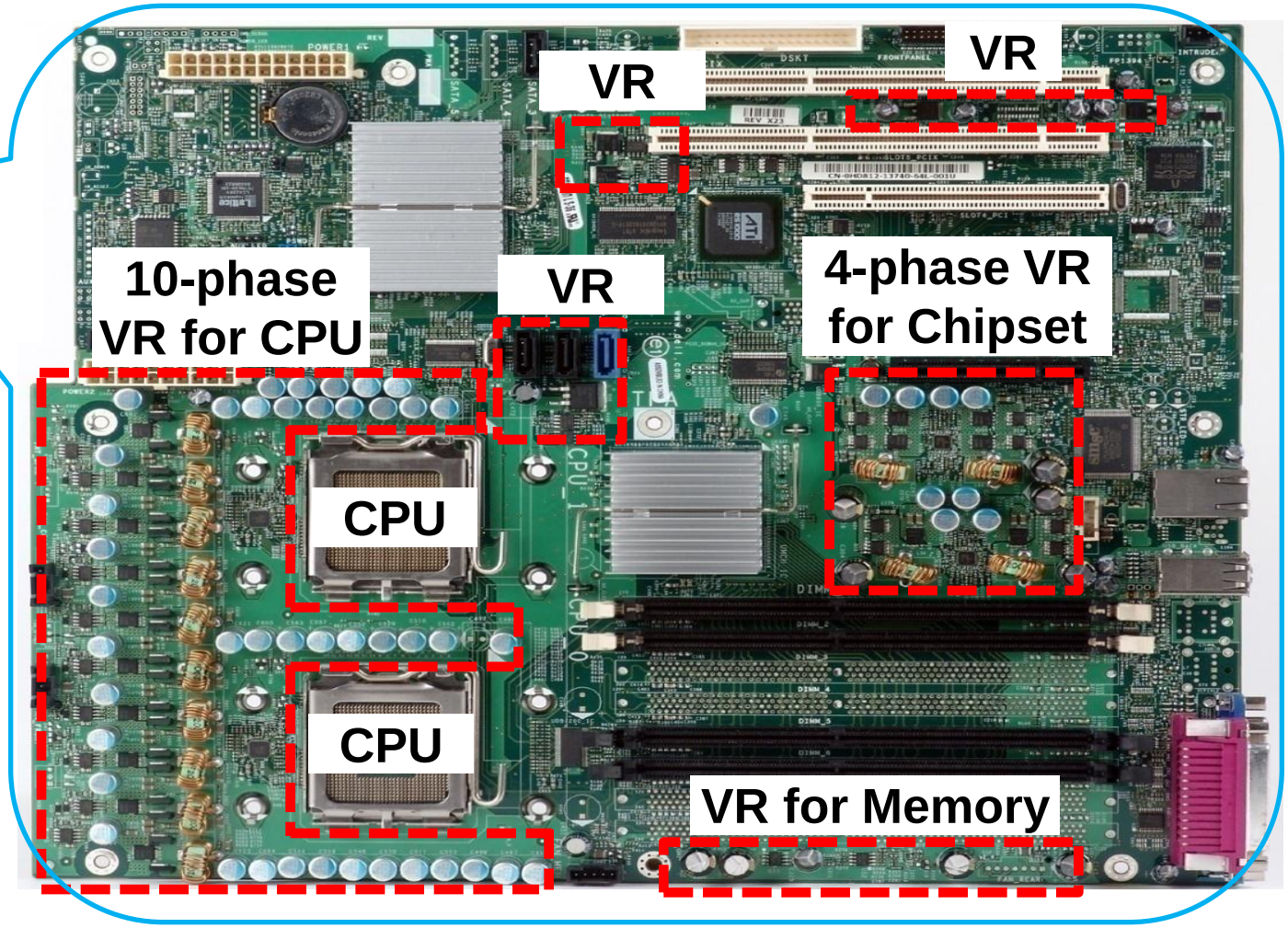
Network

Desktop

Today's Server Motherboard



Server

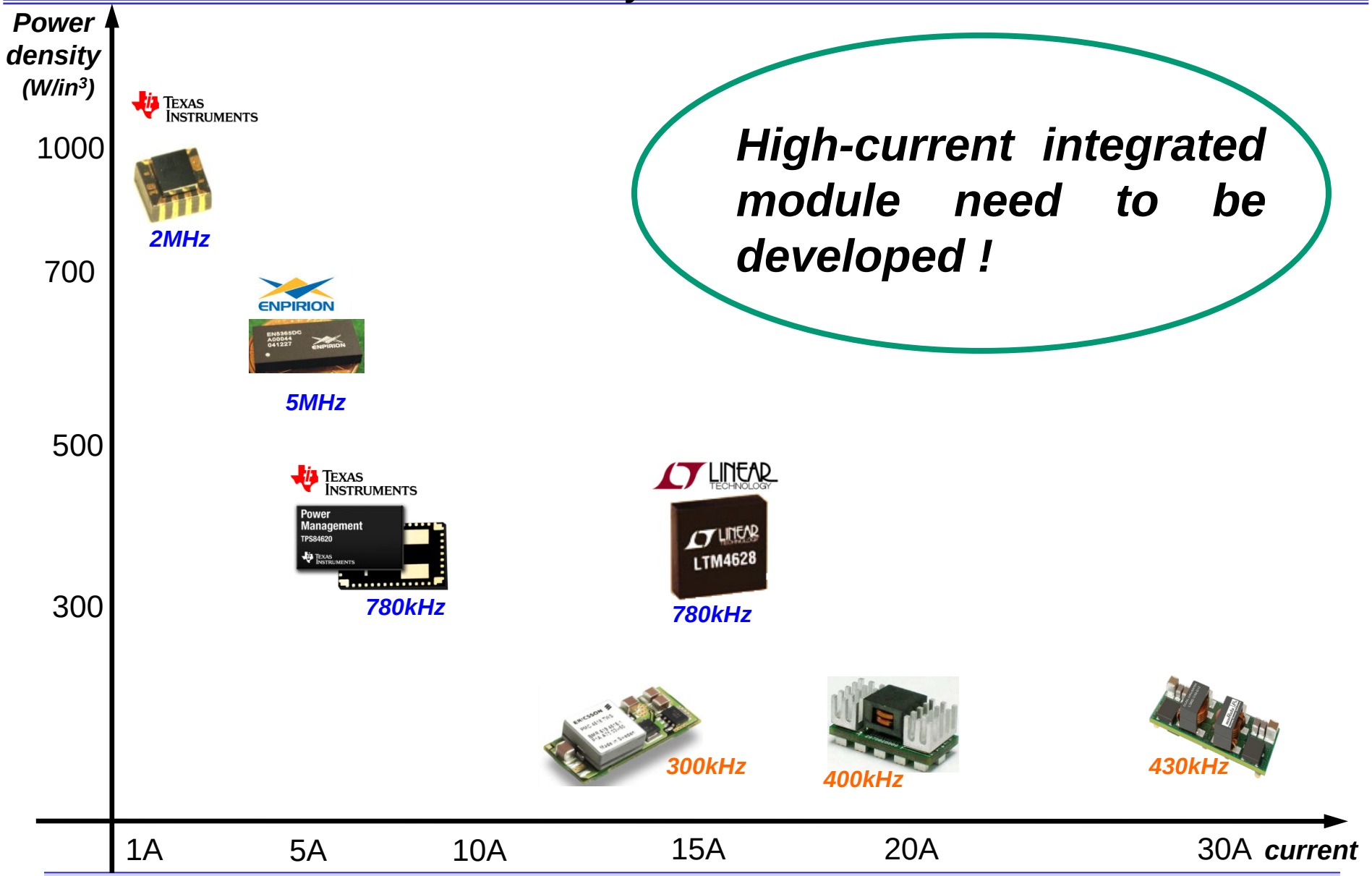


Around 30% real estate of motherboard is occupied by VR

High density power module is demanded

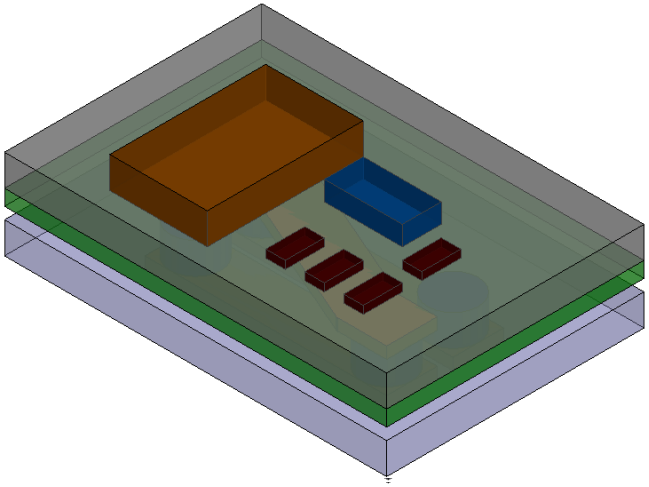
Power Density of POLs

- Industry State-of-the-art



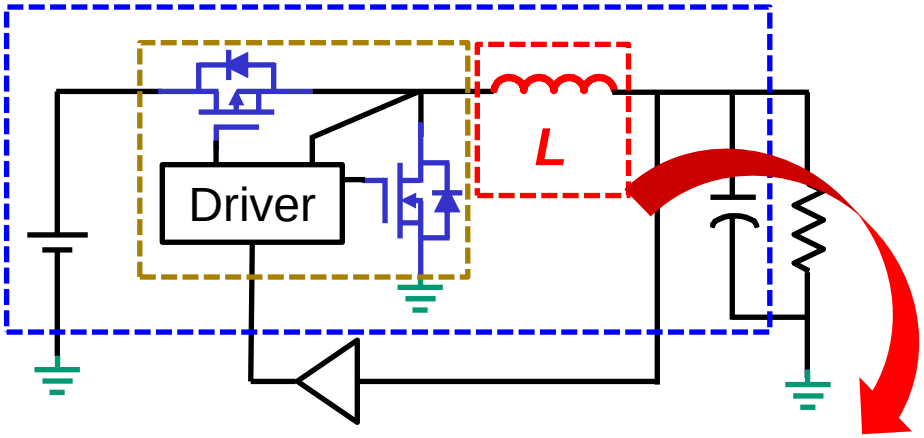
High-current integrated module need to be developed !

Objective

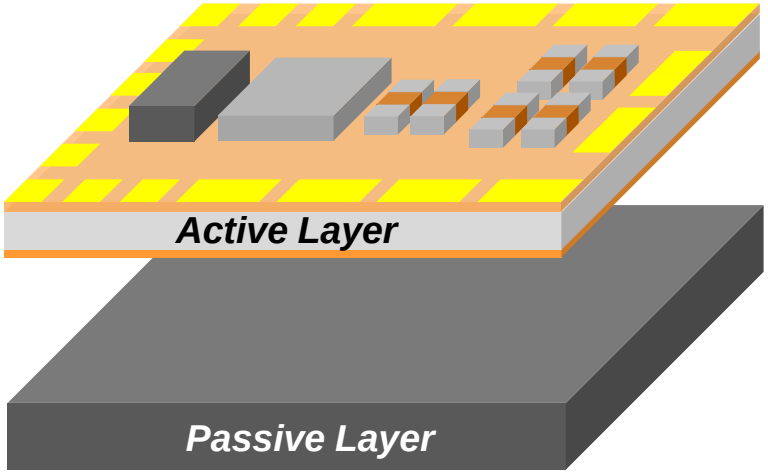


- High-Density High-Current Module (>1000 W/in^3@ >10A)
- High Switching Frequency (2 ~ 5 MHz)
- High Efficiency (88%)
- 3-D Integration
- IR Generation 1.1 GaN Device
- New Magnetic Material

3D Integrated POL Converter



3D Integrated Converter



Active Layer:

Switches, driver, input/output capacitors

2 Layer DBC Substrate (better thermal)

Multi-Layer PCB Substrate (low cost)

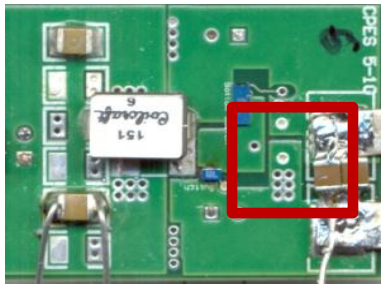
Passive Layer:

Low profile inductor substrate

Benefit: Footprint saving and fully utilize space

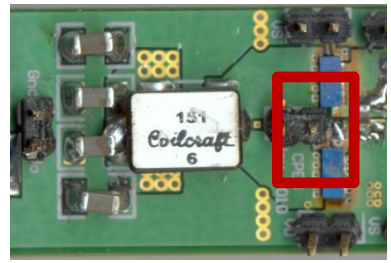
POL Modules with Discrete GaN

CPES Gen 1



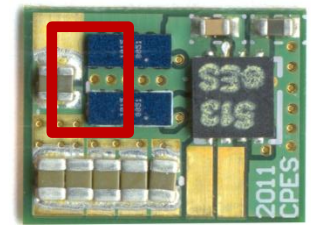
L_{Loop}=6.30nH

CPES Gen 2



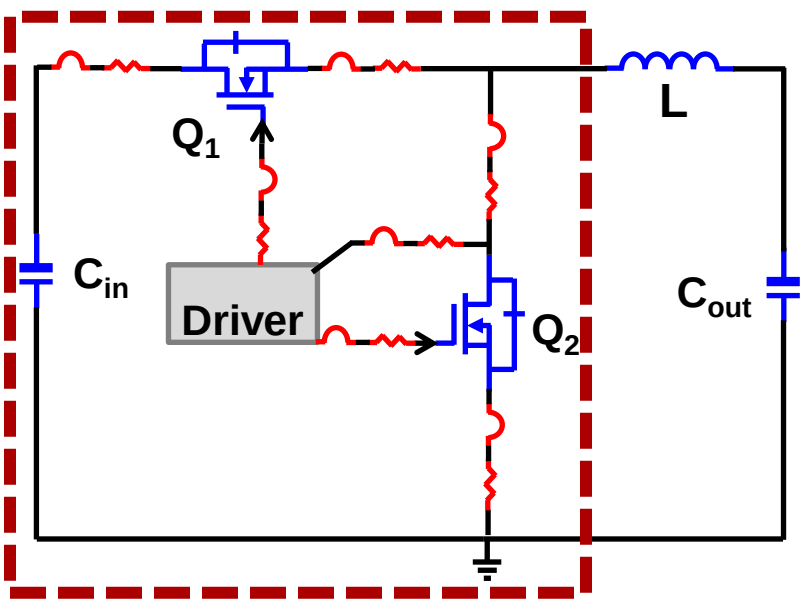
L_{Loop}=2.90nH

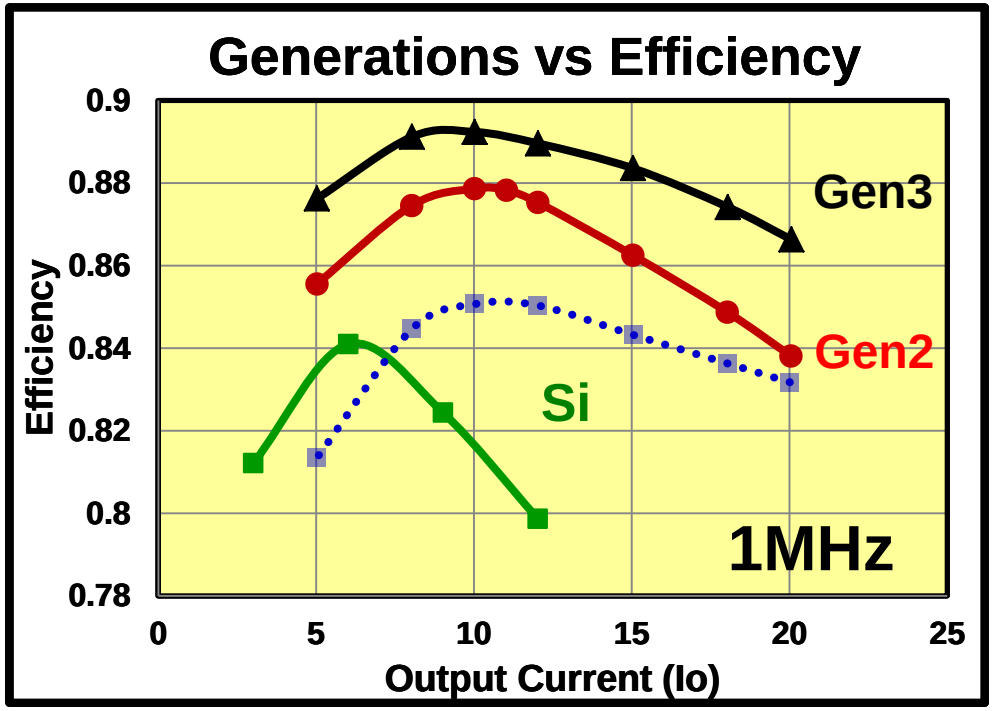
CPES Gen 3



L_{Loop}=1.19nH

Parasitic Loop Inductance (L_{Loop})



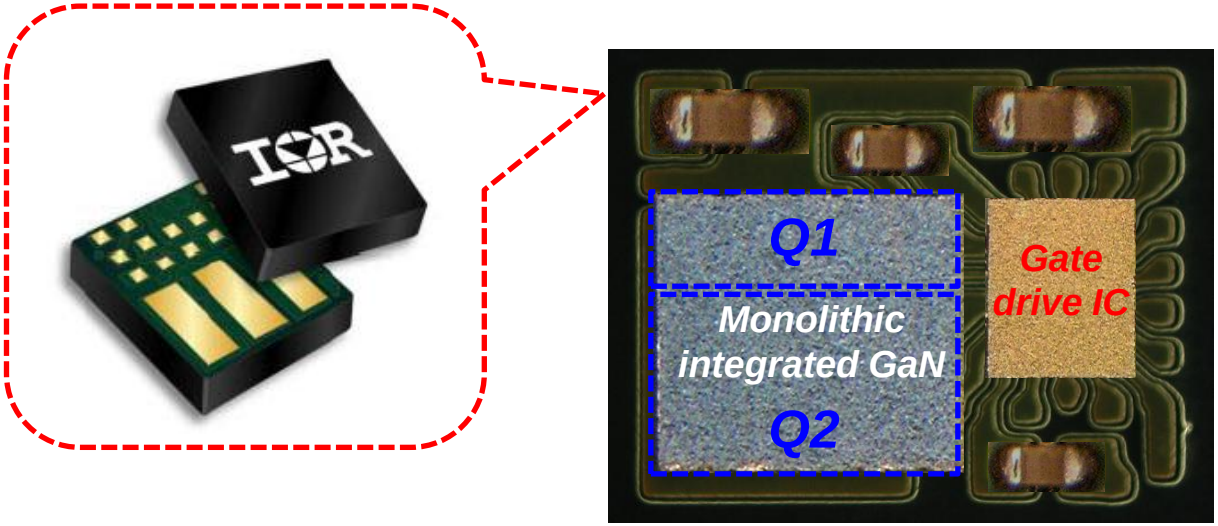


[1] D. Reusch, F. C. Lee, D. Gilham, and Y. Su, "Optimization of a High Density Gallium Nitride Based Non-Isolated Point of Load Module," ECCE, 2012.

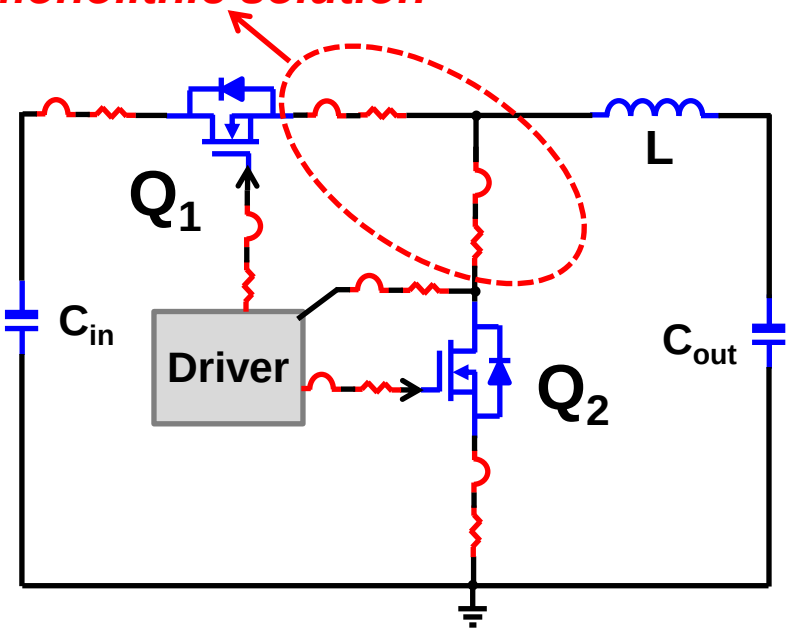
IR GaN: Monolithic Solution

iP2010 & iP2011 GaN Module

Integrated Power Module with Driver

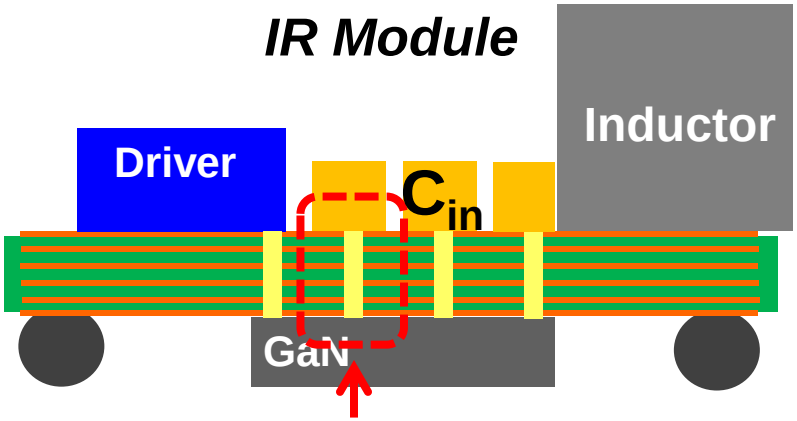


Minimized with monolithic solution



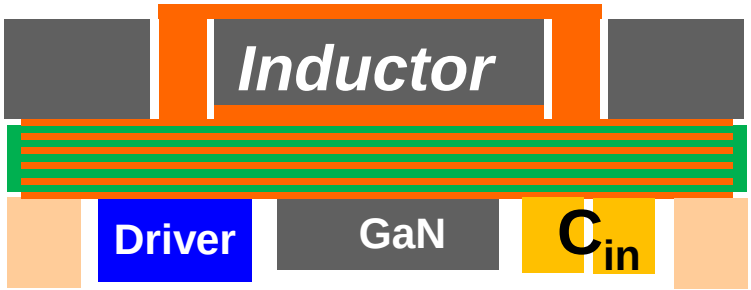
- *Integrated design minimizes the parasitics;*
- *Drive signals are tuned to provide slightly overlap below the threshold voltage;*
- *More suitable for high frequency.*

1st Modification : Power Module Layout

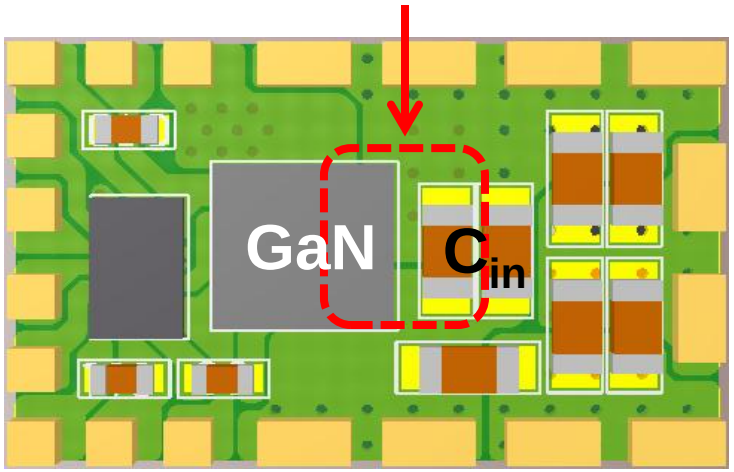


L_{Loop} = *0.1 nH*

(Extremely small)



L_{Loop} = *0.9 nH*



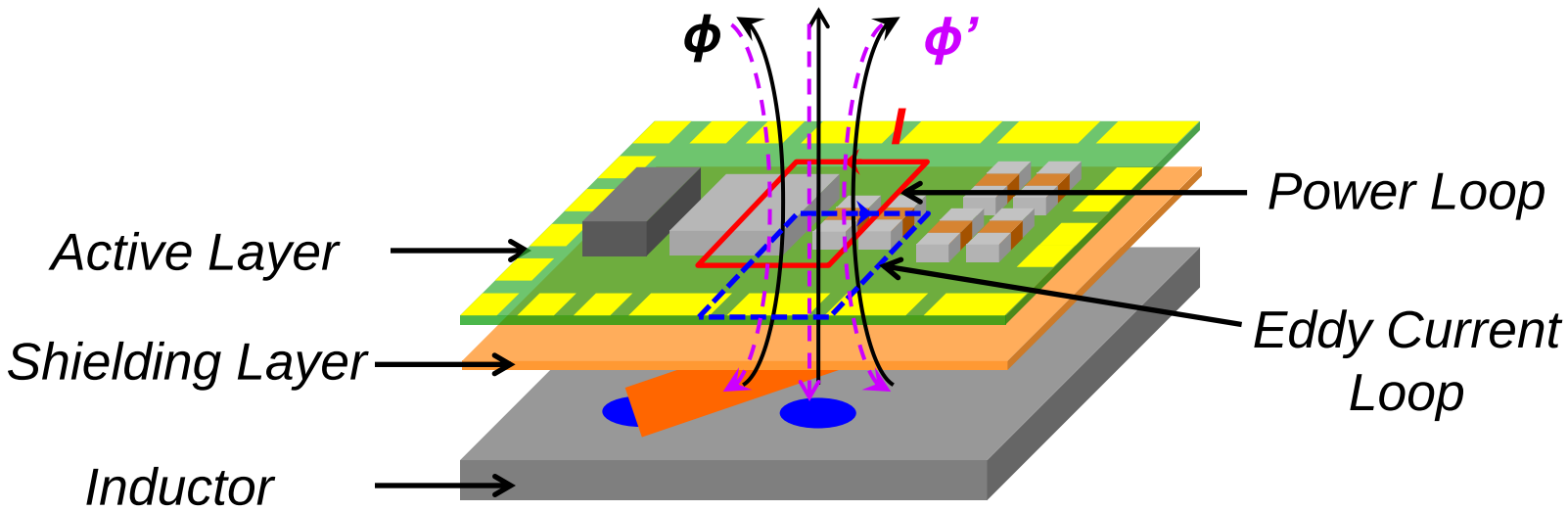
Bottom View of CPES Module

CPES Module

- Integrated Inductor
- Larger parasitic inductance

[2] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," ECCE ,2012.

2nd Modification: Adding Shielding Layer

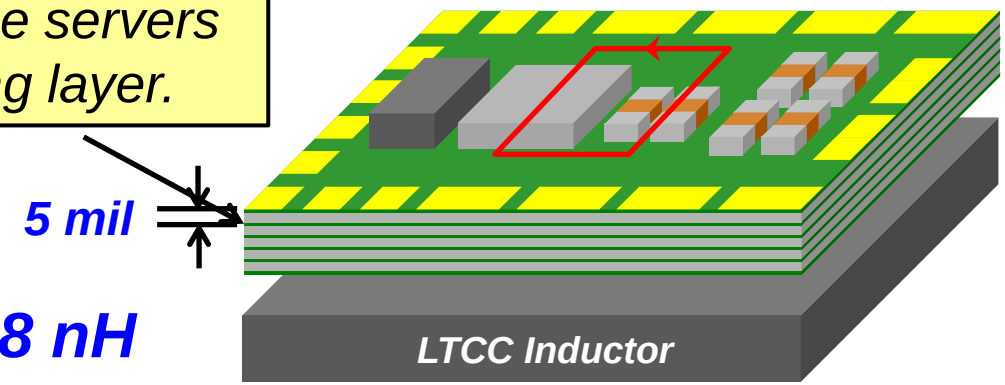


- **Loop inductance is reduced by using shielding layer.**

[2] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," ECCE ,2012.

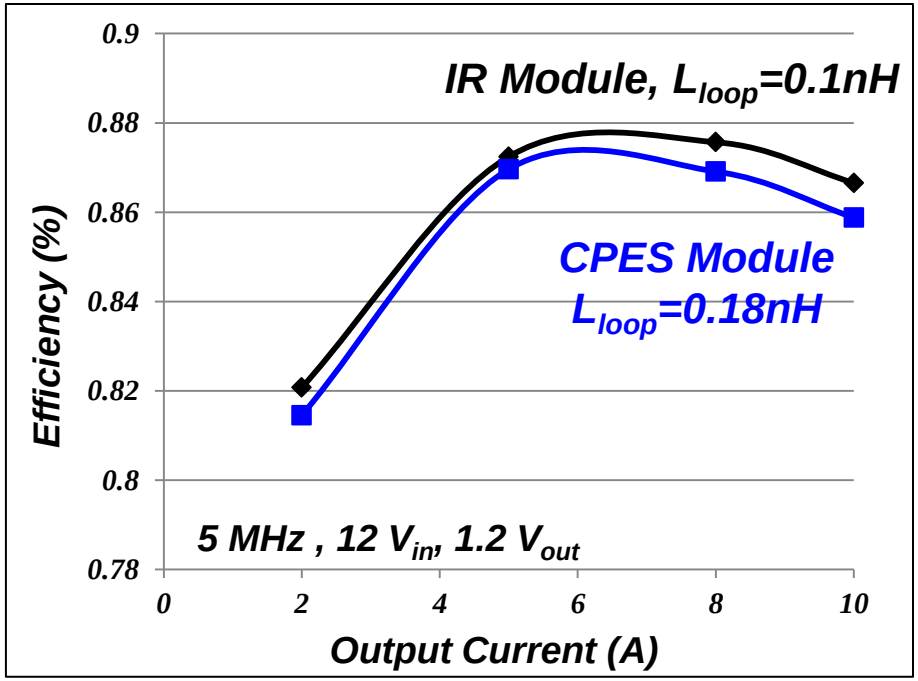
Using Ground Plane as Shielding Layer

Ground plane servers as shielding layer.



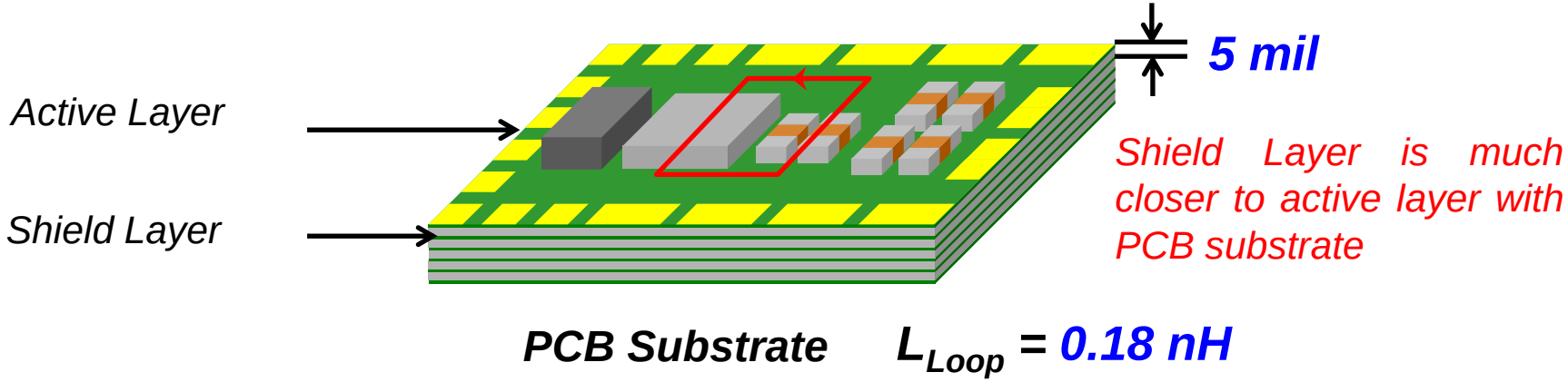
Six Layers PCB Substrate

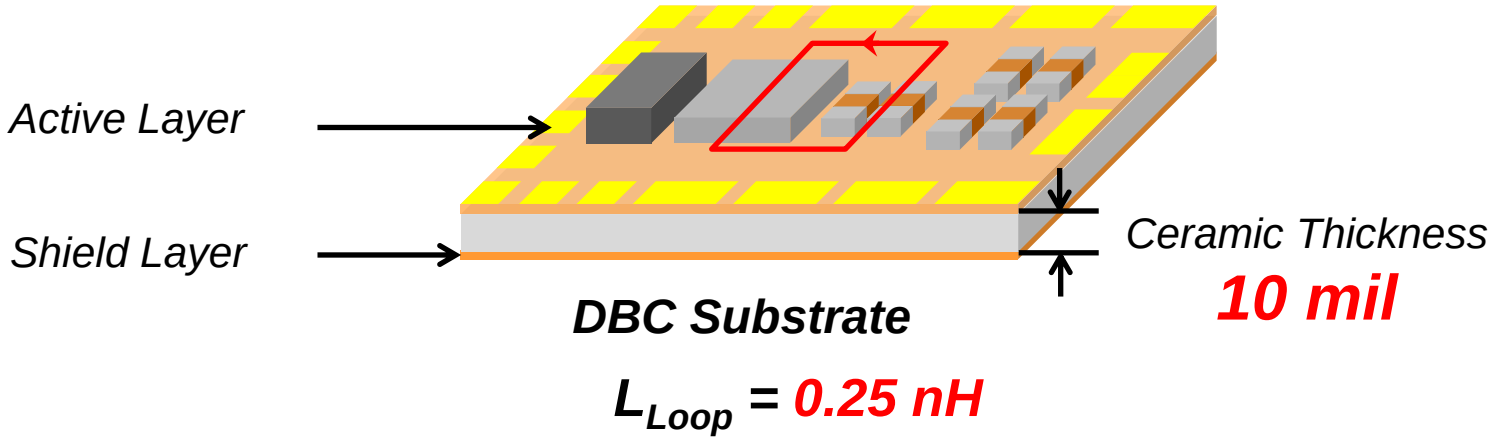
L_{Loop} = **0.18 nH**



[2] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," ECCE, 2012.

Loop Inductances of DBC Substrate

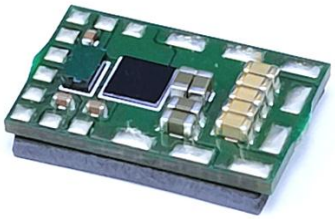




- DBC ceramic thickness is usually 10 to 40 mil, therefore the shielding layer has less field cancellation effect.

[2] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," ECCE, 2012.

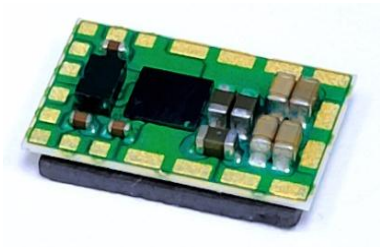
Efficiency of PCB & DBC Modules



PCB 1-Phase Module

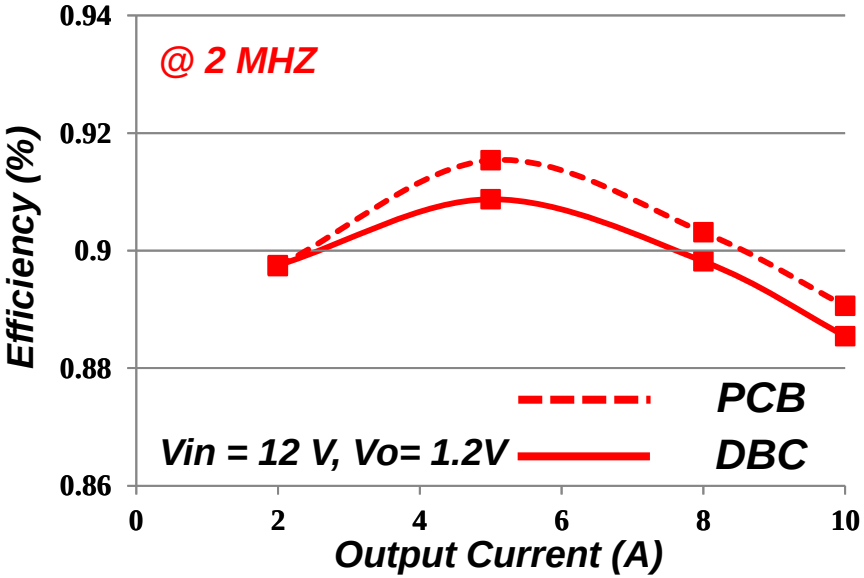
L_{Loop} = 0.18 nH

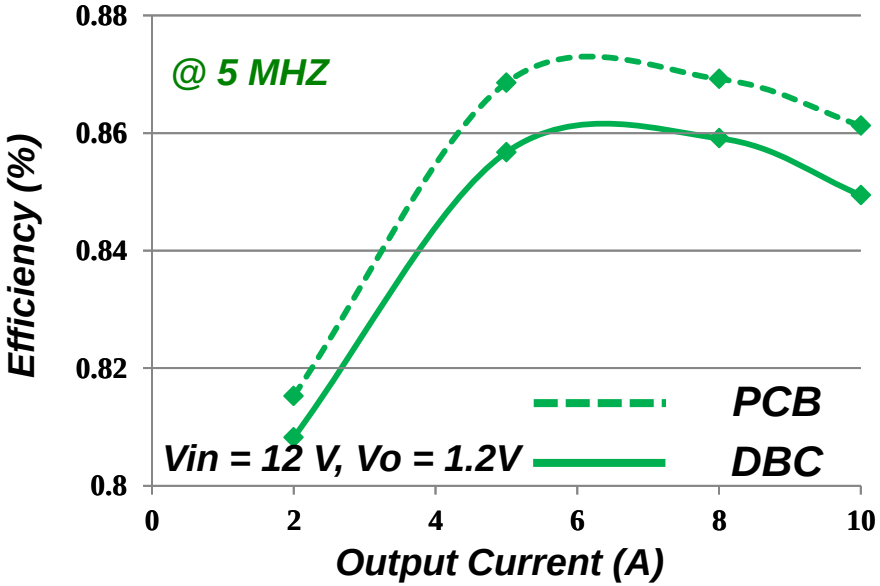
Vs.



DBC 1-Phase Module

L_{Loop} = 0.25 nH



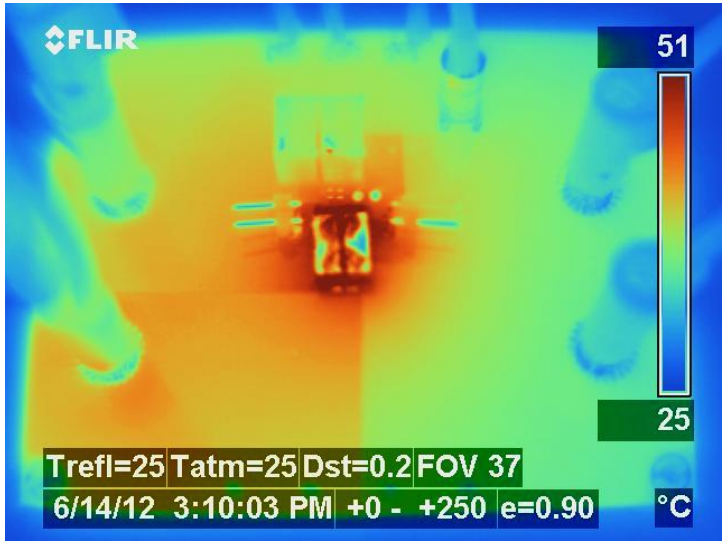


- DBC has 0.5-1% lower efficiency than PCB version duo to higher L_{LOOP}.

[2] S. Ji, D. Reusch, and F. C. Lee, "High frequency high power density 3D integrated Gallium Nitride based point of load module," ECCE, 2012.

Thermal Comparison for PCB & DBC Modules

Vin = 12V, Vout = 1.2V, Fs = 5MHz, T_A = 21 °*C, No Air Flow*



PCB Substrate

Io = 10A , P_{Loss} = *2.2W*

T_{GaN} = 67.5 °C, T_{Driver} = 54.5 °C

Io = 15A , P_{Loss} = *3.26W*

T_{GaN} = 97 °C, T_{Driver} = 76.1 °C

DBC Substrate

Io = 10A, P_{Loss} = *2.35W*

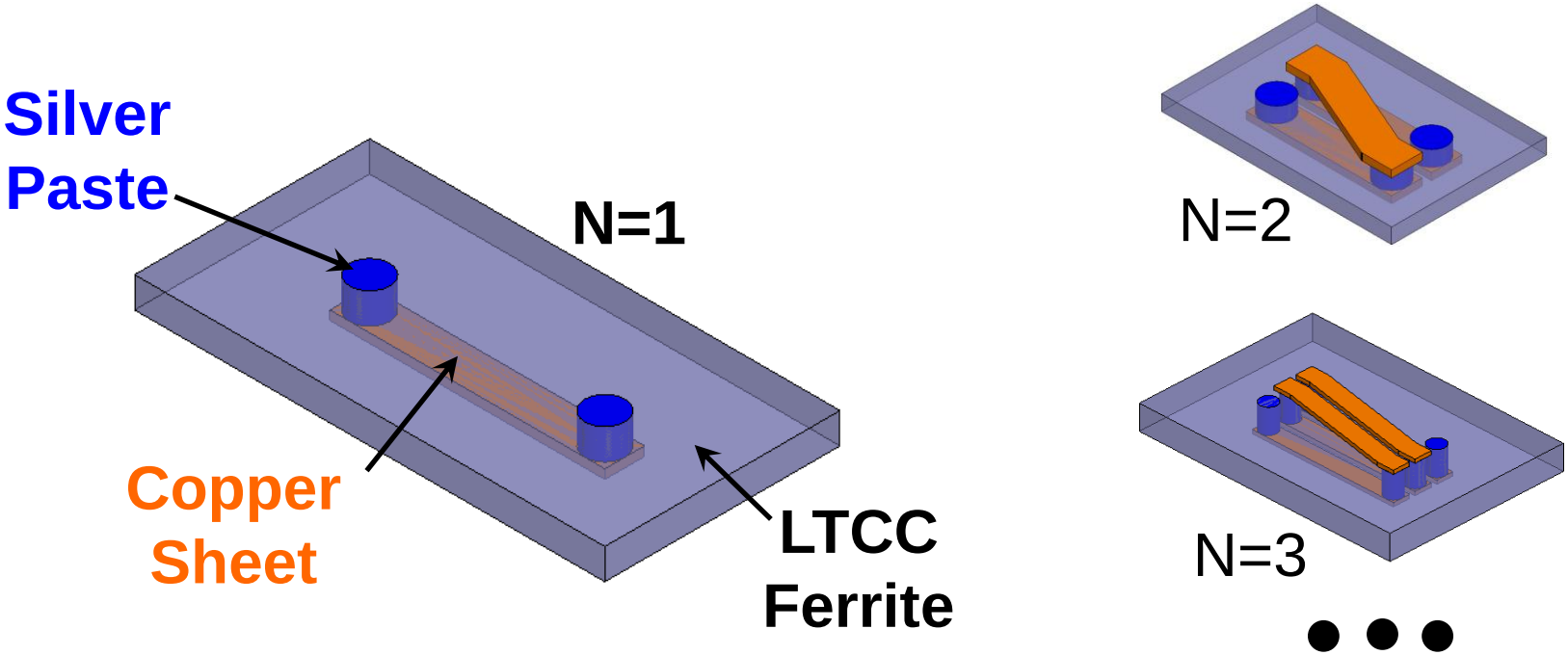
T_{GaN} = 63.3 °C, T_{Driver} = 51.5 °C

Io = 15A, P_{Loss} = *3.37W*

T_{GaN} = 82.9 °C, T_{Driver} = 72 °C

- DBC module has better thermal performance than PCB module.

LTCC Inductor for 3D Integrated Module

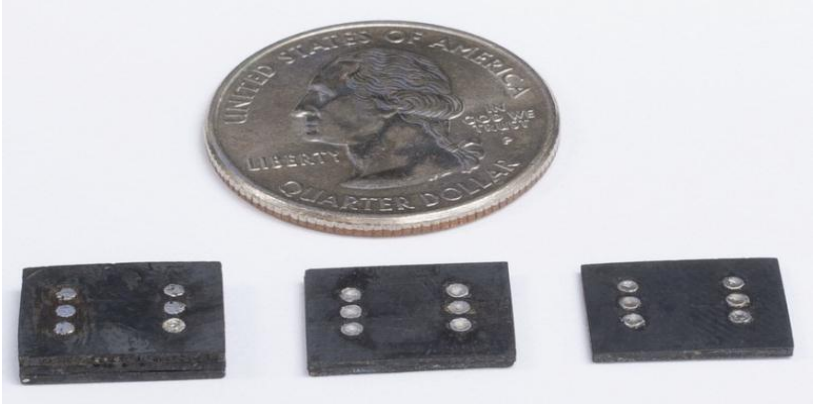


LTCC – Low Temperature Co-fired Ceramics

- *Good high frequency performance.*
- *Enable low profile inductor fabrication.*

[3] Q. Li and F. C. Lee, "High Inductance Density Low-Profile Inductor Structure for Integrated Point-of-Load Converter," APEC, 2009.

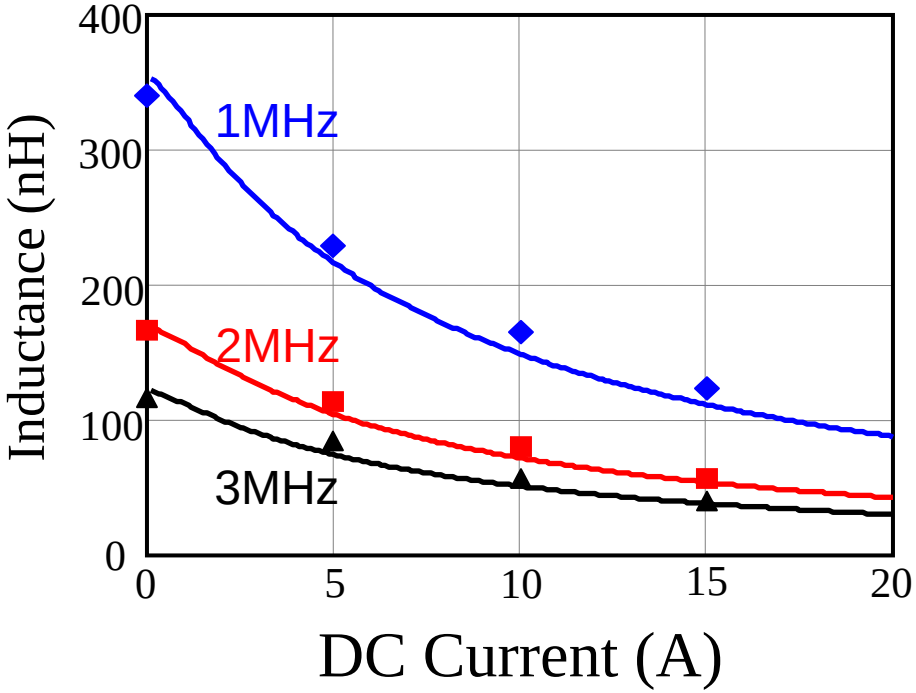
Inductance with Different DC Current



120 nH
for 1 MHz

60 nH
for 2 MHz

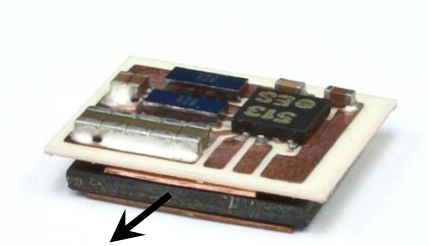
40 nH
for 3 MHz



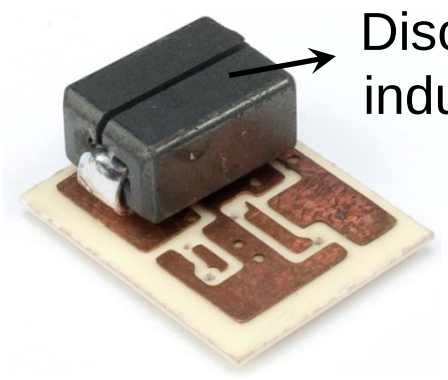
- LTCC inductors have the non-linear inductance characteristics.

[4] Y. Su, Q. Li, M. Mu, D. Gilham, D. Reusch, and F. C. Lee, “Low profile LTCC inductor substrate for multi-MHz integrated POL converter,” APEC, 2012.

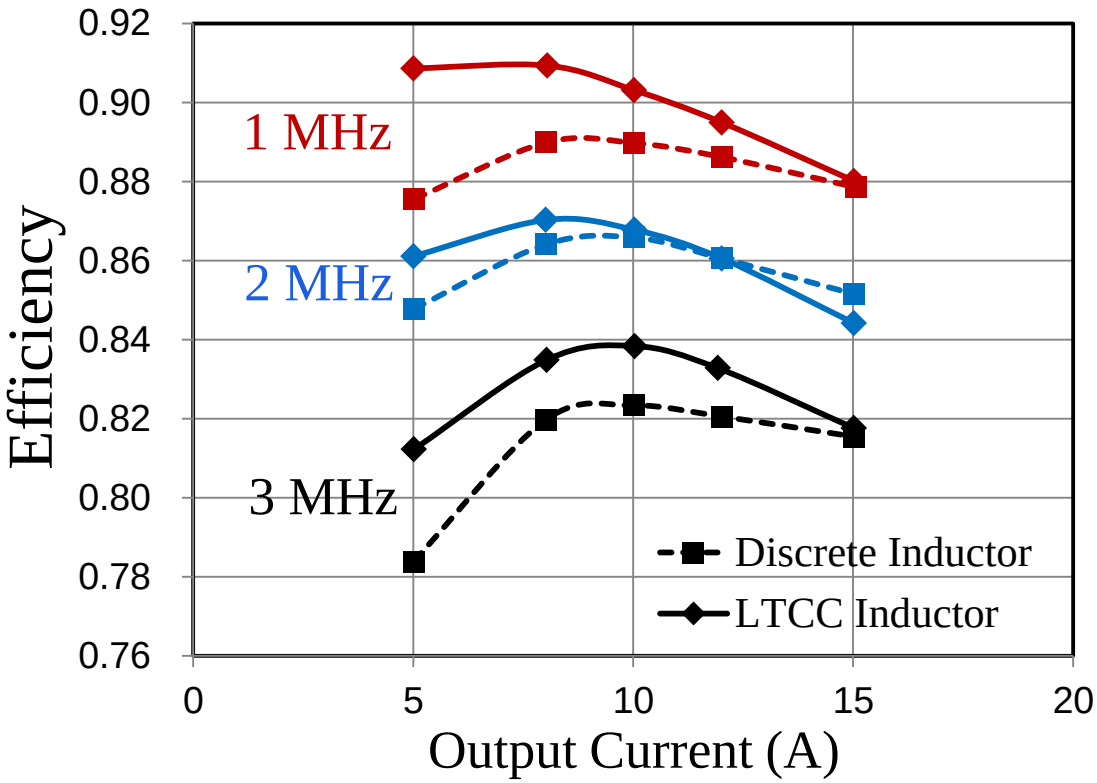
Efficiency with Different Inductors



LTCC inductor substrate



Discrete inductor



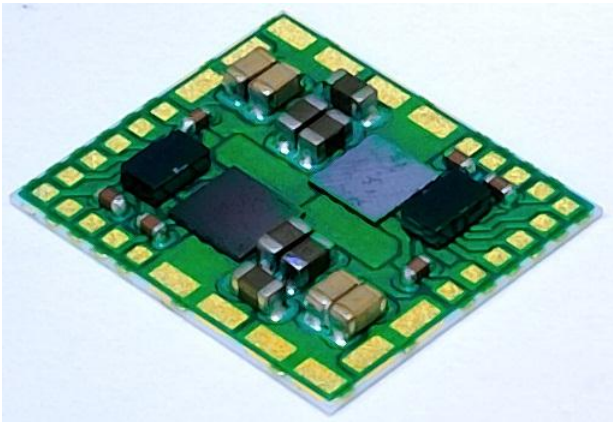
With low profile LTCC inductor

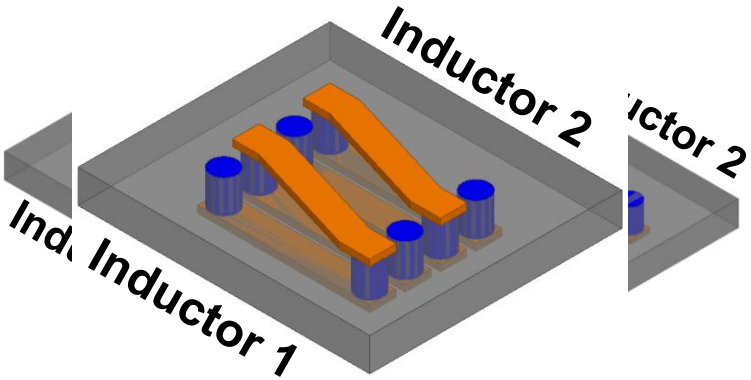
- Higher power density
- Higher light-load efficiency

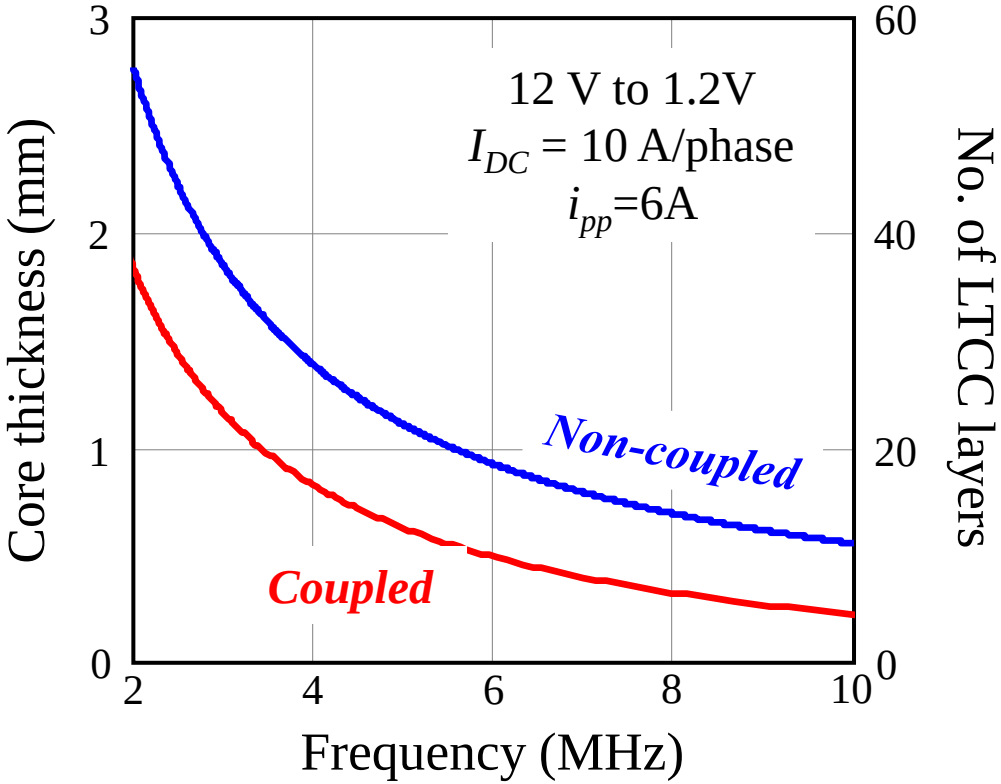
[4] Y. Su, Q. Li, M. Mu, D. Gilham, D. Reusch, and F. C. Lee, "Low profile LTCC inductor substrate for multi-MHz integrated POL converter," APEC, 2012.

Two-Phase Module with Coupled Inductor

2-Phase Module





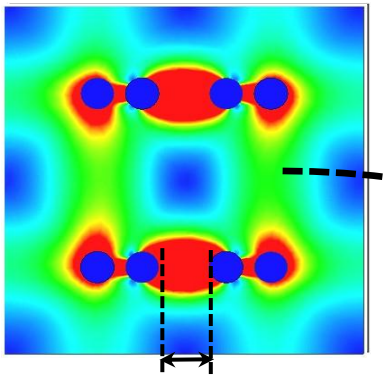


- With coupled inductor, more than 40% core thickness reduction can be achieved.

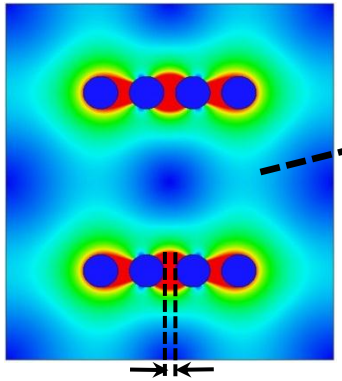
[2] & [5] Q. Li, Y. Dong, F. C. Lee, and D. Gilham, "High-Density Low-Profile Coupled Inductor Design for Integrated Point-of-Load Converters," *IEEE Trans. Power Electron.*, vol.28, no.1, pp.547-554, Jan. 2013.

The Impact of DC Flux Cancellation
on LTCC Coupled Inductor

Coupled L I_{DC}=10A

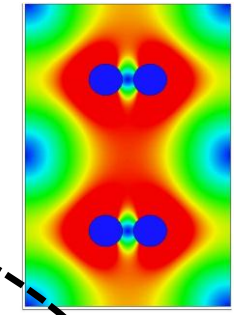


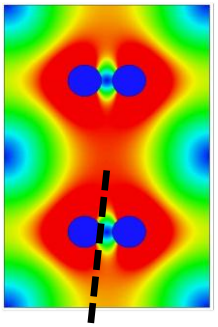
$|\alpha| = 0.3$ ***d* =1.8 *mm***

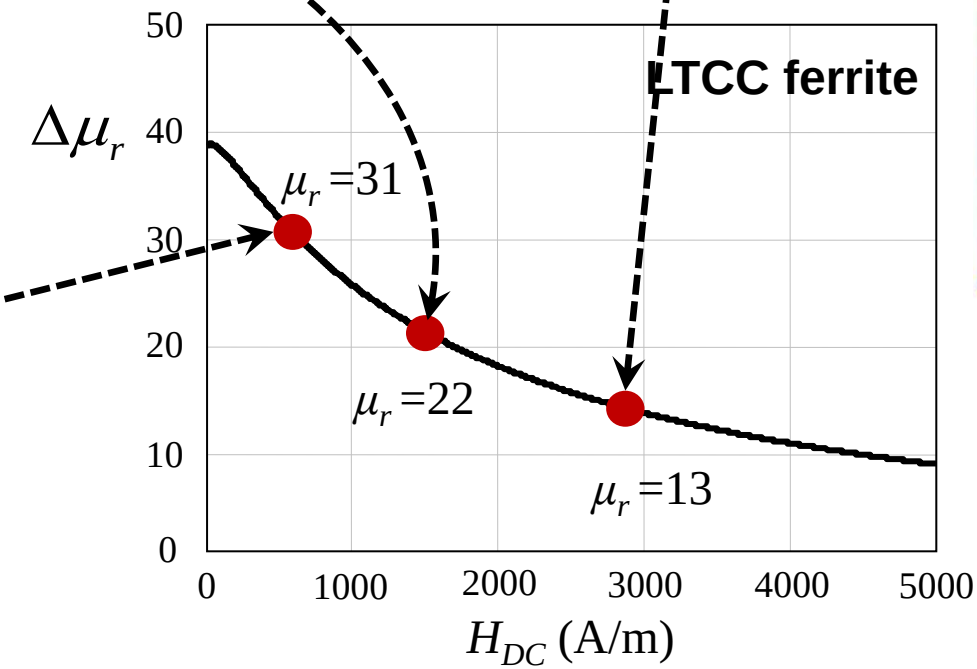


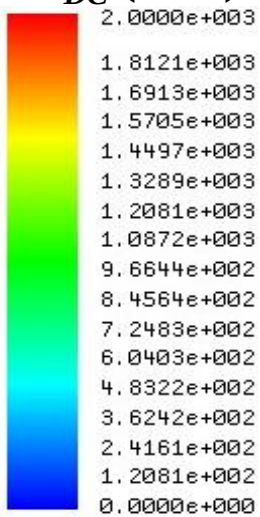
$|\alpha| = 0.5$ ***d* =0.4*mm***

Non-Coupled L I_{DC}=10A



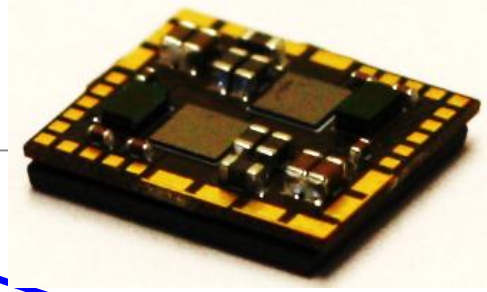


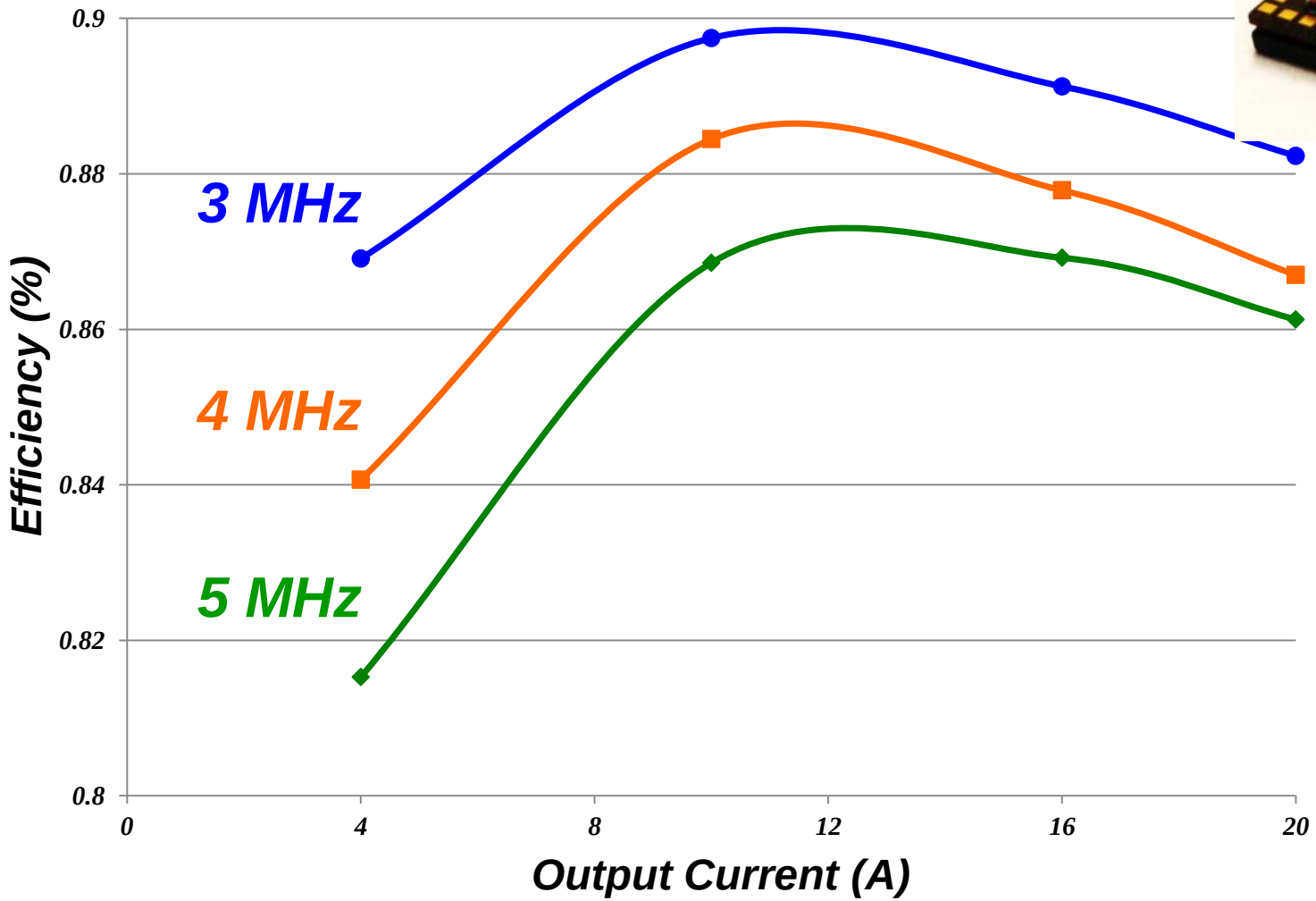




- ❑ **Cancel DC flux**
- ❑ **Increase μ_r**
- ❑ **Reduce core thickness**

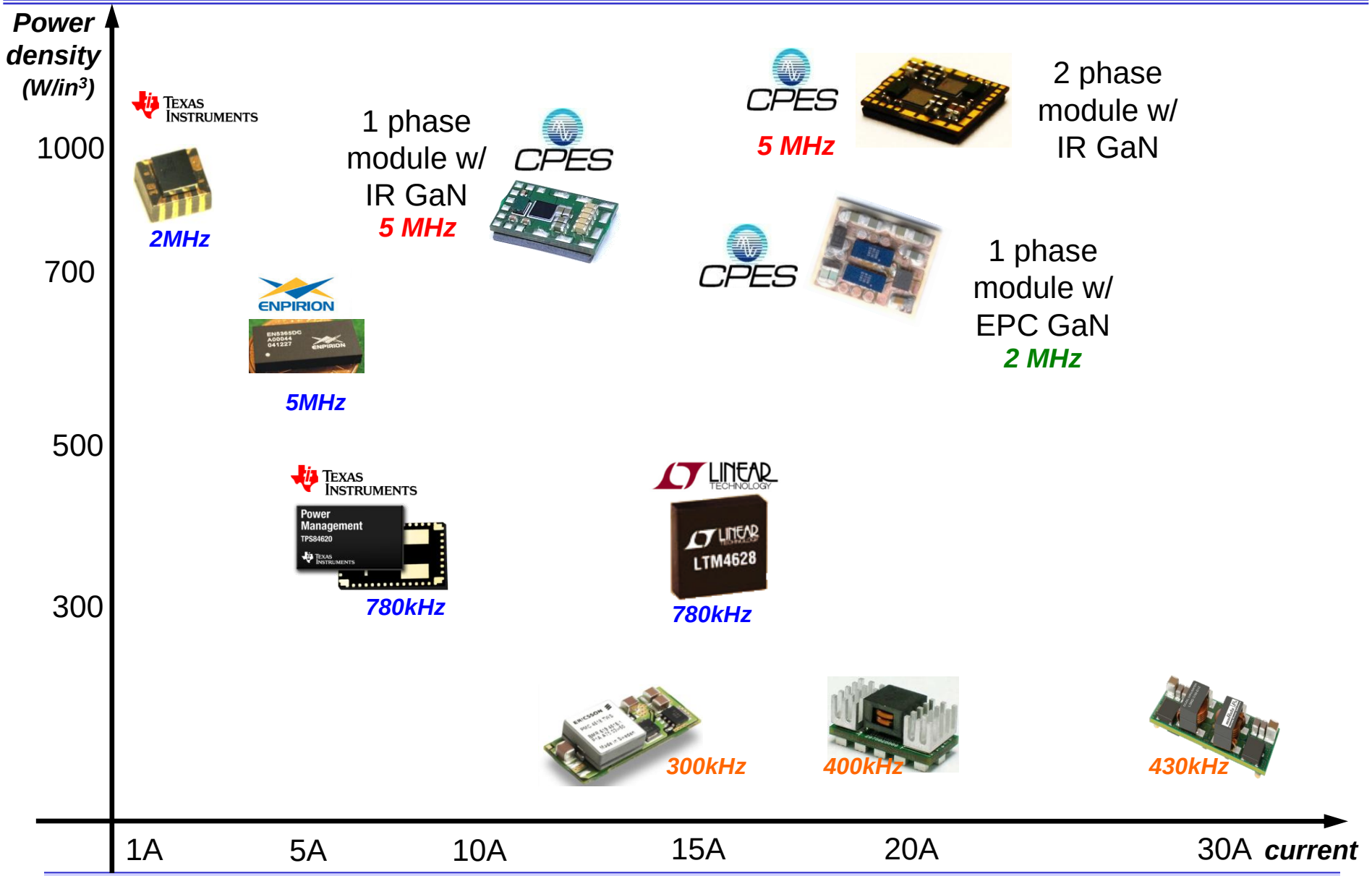
Efficiency of 1.2V PCB Two Phase Module





PCB 2 Phase Module

Power Density Achievement



Thank You !