Thermal Management at Nanoscale: Problems and Opportunities

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Nano-Device Laboratory (NDL)
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Profile: experimental and theoretical research in nano materials and devices

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Thermal and Electrical Characterization

Device Design and Characterization

Raman, Fluorescence and PL Spectroscopy

Direct Energy Conversion

Bio-Nanotech

Optoelectronics

Electronic Devices and Circuits

Theory and Modeling

Nanoscale Characterization

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Outline

- Motivations
  - Downscaling and the thermal issues
  - High-power density electronics and heat removal
  - New approaches for thermal management
  - High-heat-flux method and hot-spot spreading

- Thermal Conductivity of Graphene
  - New non-contact measurement technique
  - Graphene vs carbon nanotubes

- New possibilities

- Conclusions
The Thermal “Show Stopper” for Electronics

IEEE Spectrum illustration of the thermal issues in the feature article

A.A. Balandin, Chill Out: New Materials and Designs Can Keep Chips Cool (October 2009)

No BIG fan solutions!

The old industry approach does not work

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Trends: Increase in Thermal Design Power

Thermal design power is the maximum sustained power dissipated by the microprocessors. TDP was increasing with increasing performance complicating thermal management. The switch to multi-core designs.

Data is after R. Mahajan et al., Proceed. IEEE (2006)

The problem of hot spots:
- Non-uniform power densities
- Power densities above 500 W/cm²
**ITRS: Thermal Management Issues**

→ IC performance is now limited by the power, which can be dissipated without exceeding the maximum $T$ set by the reliability requirements.

→ **ITRS:** power consumption, both dynamic and static, related to unavoidable leakage currents, is an urgent challenge.

→ In the next five years up to 80% of microprocessor power will be consumed by the interconnect wiring (compare to 51% at 130 nm node).

→ Power dissipation in the interconnect structure will increase dramatically due to higher clock frequencies and increase in the number of metal layers and interfaces.

→ Joule heating in the interconnects may result in significantly higher temperature rise as compared to power dissipated in active devices.
New Aspects of Thermal Transport in Nanoscale Devices and Circuits

Technology Trends:
- Increasing number of interconnects
- Increasing power density
- Increased leakage current
- High switching frequencies
- Increased thermal resistance of the chip
- Thermal boundary resistance
- Materials with low thermal conductivity

Device Feature Sizes
- CMOS gate length < 50 nm
- CMOS gate-oxide thickness ~ 1.2 nm
- Superlattice period: ~ 1.5 nm

New Phenomena at Nanoscale:
- Acoustic phonon MFP in bulk crystalline Si at T=300K (Debye model): ~ 50 nm
- Comparison: electron MFP in Si: 7.6 nm
- Dominant phonon wavelength in Si: 1.4 nm at T=300 K or 4 mm at T=0.1 K

Nanostructured materials do not conduct heat as well as bulk materials

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Thermal Issues in High-Power Density Electronics: GaN FETs

Strategy: Incorporation of the thermal management constrains early at the device design stage

The “Nano-Problem”: Thermal Conductivity Degradation at Nanoscale

Thermal conductivity definition:

\[ \frac{Q}{A} = -kNT \]

*RT thermal conductivity values for important materials:*

- Si: 145 W/mK
- SiO\(_2\): 1-13 W/mK
- GaN: 150-300 W/mK
- Diamond: 1000 – 2200 W/mK
- Graphite: 200 – 2000 W/mK
- CNTs: 3000 – 3500 W/mK


- Phonon - boundary scattering
- Phonon spectrum changes
Composite Substrates: Diamond Materials For Hot Spot Spreading

New Developments:

→ Si wafers become thinner (consider the effects on the Si cost of the rapid developments in solar cells)
→ Progress in synthetic diamond deposition and growth
→ Diamond heat spreaders will be closer to heat generation areas in thinned Si wafers

Issues:

→ Compatibility with Si CMOS
→ Cost
→ Finding an optimum combination of material properties: grain size vs thermal conductivity vs. interface quality vs. temperature of deposition
Finding the Optimum Synthetic Diamond - Si Combination

Nanocrystalline diamond offers smoother interface but lower thermal conductivity.

- Hopping Model (22nm, t=0.32)
- Hopping Model (26nm, t=0.2)
- Hopping Model (2μm, t=0.9)
- Minimum K for Carbon
- Bulk Diamond: Callaway Model

Minimization of the thermal boundary resistance (TBR)
New Unique Material Option: Graphene

Individual atomic layers of sp²-hybridized carbon bound in two-dimensions. Crystalline graphite is composed of graphene layers.

“Unrolled Carbon Nanotube”

“Graphene Revolution” brought about by K.S. Novoselov and A.K. Geim (Manchester, UK and Chernogolovka, Russia) with the help of bulk graphite and something similar to a Scotch tape.


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Practical Applications of Graphene: Transistors and Interconnects


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Prospects of the High-Heat Flux Thermal Management with Graphene

- Concept change: from the post-chip making level to the device and materials level consideration at nanoscale

- Passive high-heat flux thermal management at the device/chip level

Issues:
- Insulator vs conductor
- Anisotropy
- Thermal expansion
- Temperature stability
- Large-area

Possible Material Systems:
- Synthetic diamond
- Carbon nanotubes
- Graphene
Conventional Measurement Techniques Do Not Work for Graphene

**3-ω Thermal Conductivity Setup**

Cr/Au heater-thermometer sensors patterned on top of the samples by photolithography.

**Transient Plane Source Technique**

- **TEMPERATURE RISE (°C)**
- **TIME (s)**

- Dissipated Power
  - Sample: 0.05 W
  - Si Wafer: 0.5 W

- Measurement Time: 5 s

**Laser – Flash Technique**

Thermal conductivity and heat capacity extraction from the T(t) dependence.
Micro-Raman Spectroscopy of Graphene

Alternatives:
- low-temperature transport study
- cross-sectional TEM

Disorder D band: ~ 1350 cm$^{-1}$: in-plane $A_{1g}$ (LA) zone-edge

G peak: double degenerate zone center $E_{2g}$ mode

I. Calizo, A.A. Balandin et al., *Nano Letter* 7, 2645 (2007)
Raman Nanometrology of Graphene Layers

2D-band features of graphene on a standard Si/SiO$_2$ (300nm) substrate are highly reproducible and, together with the G-peak position, can be used to count the number of graphene layers.

Deconvolution of 2D band
Double-resonance model


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UCR Experiment: **Heating Up Graphene**

IEEE Spectrum illustration of the first measurements of thermal conductivity of graphene carried out at UCR.


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Experimental Approach and Suspended Graphene Layers

Graphene flakes suspended across trenches in Si/SiO₂ wafers
Extraction of the Thermal Conductivity Data: Raman Spectrometer as a Thermometer

→ Excitation laser acts as a heater: $\Delta P_G$
→ Raman spectrometer acts as a thermometer: $\Delta T_G = \Delta \omega / \chi_G$
→ Thermal conductivity: $K = (L/2a_G W)(\Delta P_G / \Delta T_G)^{-1}$

$$K = \left( \frac{L}{2a_G W} \right) \chi_G \left( \Delta \omega / \Delta P_G \right)^{-1}.$$
Graphene Heat Spreaders Designs for Active Devices and Interconnects

Nanoscale Phonon Engineering: New Possibilities for Improved Heat Removal

Other 2D Crystals with Van der Waals “Gaps”: Thermoelectric Applications

- Quintuple thickness: ~1 nm
- Identification: AFM, SEM, TEM
Active On-Spot Cooling of Nano-Devices

The Route to Three-Dimensional Electronics

Is Carbon the Answer?

Conclusions

- Heat dissipation is a crucial problem for nanometer scale devices and ULSI chips
- Thermal conductivity of most materials deteriorates when they are structured at nanometer scale
- There are some materials, which maintain or even improve heat conduction property at nanoscale: graphene
- Graphene can be used for hot-spot spreading in the active devices and interconnects
- Possibility for the high-power electronics: better thermal interface materials
- Concept change for thermal management: from post-chip design effort to materials/device level effort
Acknowledgements

Balandin group in front of the Nano-Device Laboratory (NDL), 2008

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