A 400 Amp fully Integrated Silicon Voltage Regulator with in-die magnetically coupled embedded inductors

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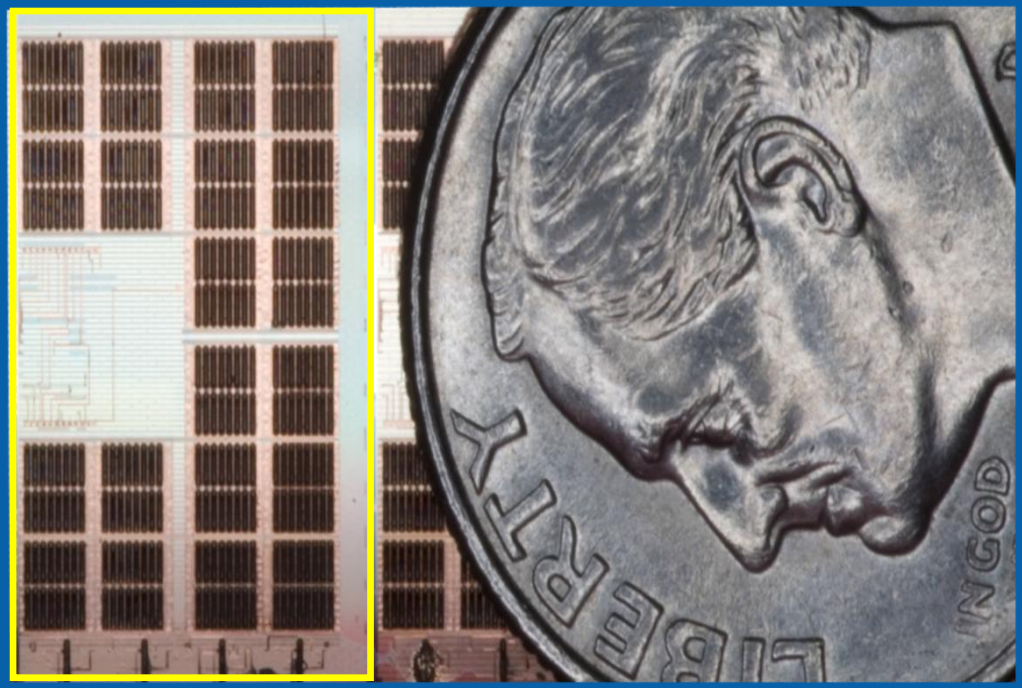
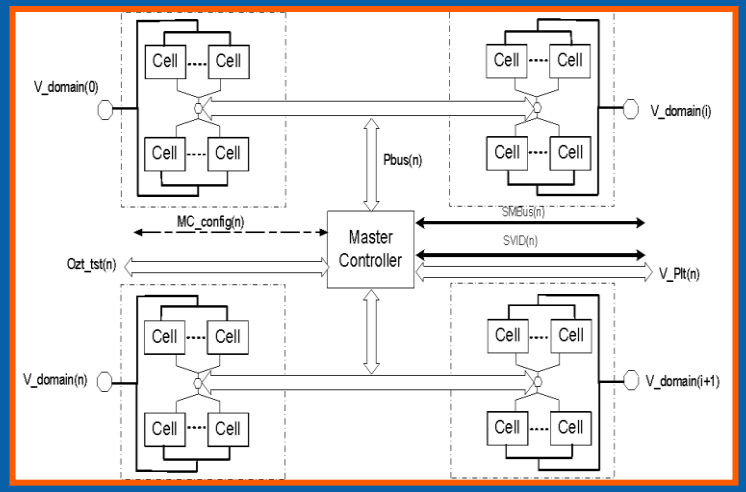
Agenda

- Architecture
- Circuits
- Results
- Conclusion

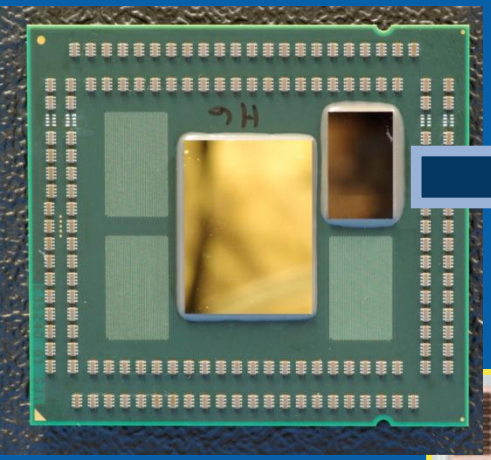


Integrated VR Technology

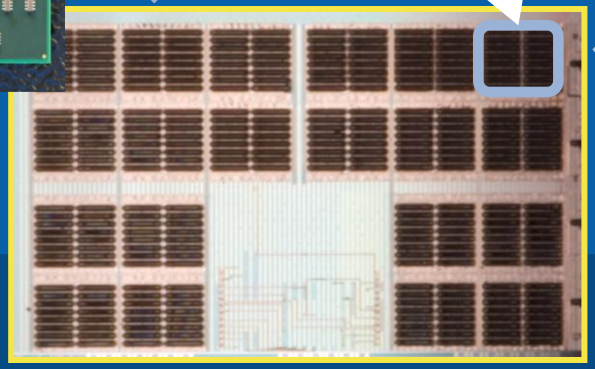
- 'Common Cell' Architecture – 20 cells
- Architecture supports flat efficiency curve
- Fine grain power management
  - Allows for multiple voltage rails
- Telemetry and Margining features
- Active Voltage Positioning for current sharing and balance
- Control features, including: JTAG, FPGA, Test/BIST



General Arch

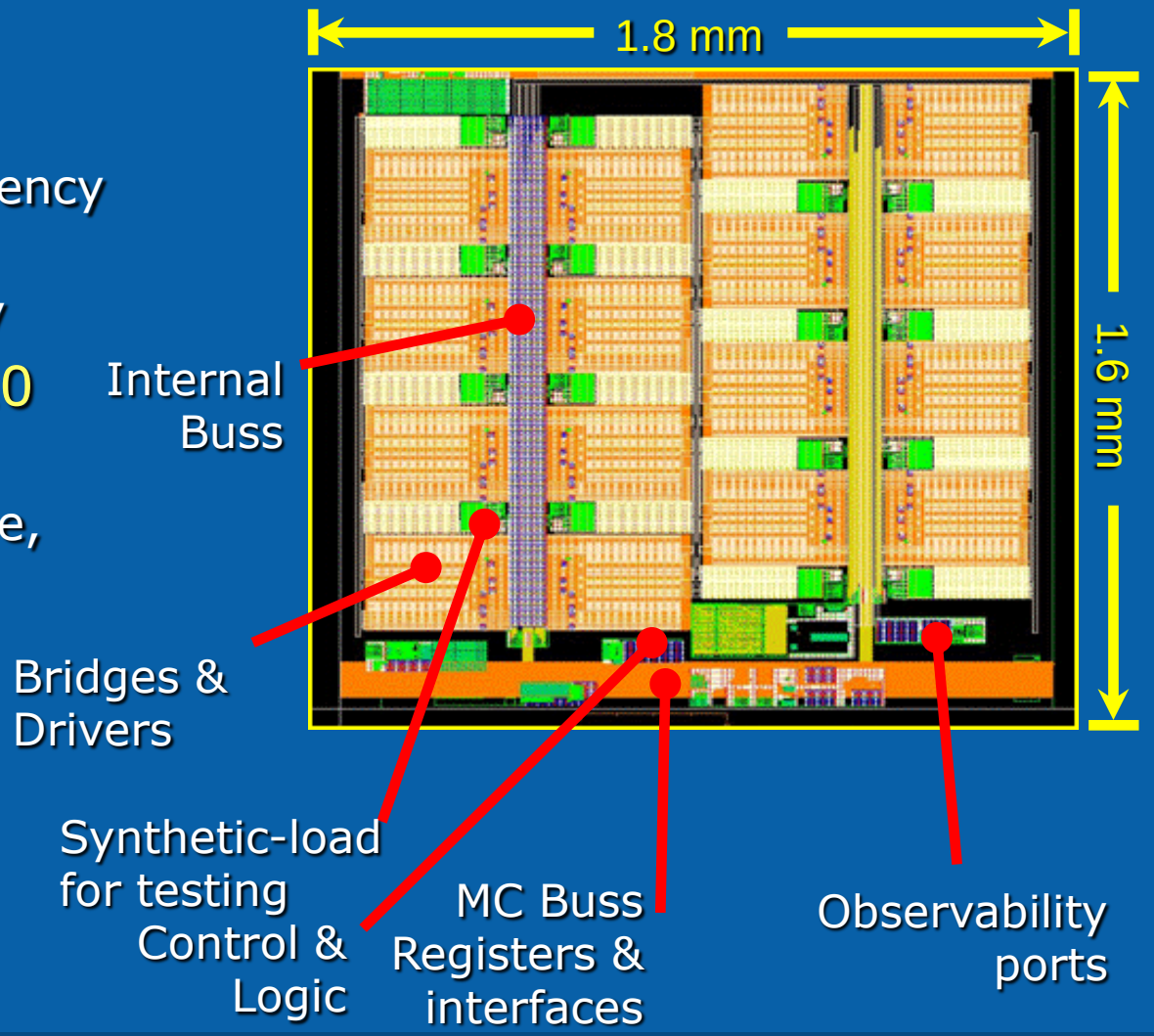


Power cell
- 2.8 mm²



Review: Power Cell Architecture

- Each Power cell = Mini VR
  - Up to 25A rating* - tested
  - Programmable switching frequency 30MHz to 140MHz
  - Ring coupled inductor topology
- 16 phases per power cell, 320 phases per chip
  - High phase count reduces noise, ripple
  - High granularity
  - Cell shedding
  - Bridge shedding
- BIST
  - Self-load and characterization system.



* Thermally constrained

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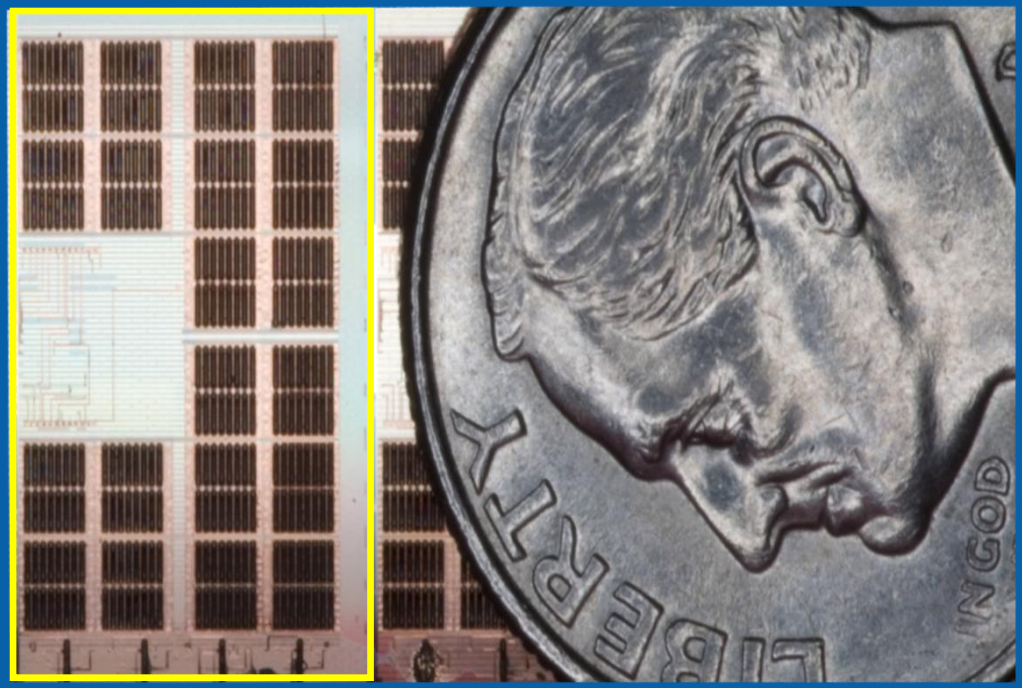
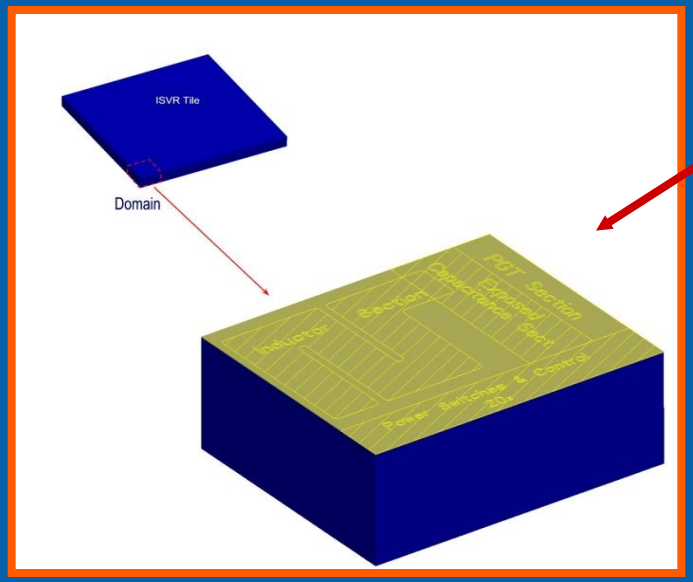
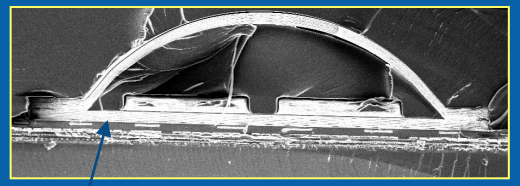


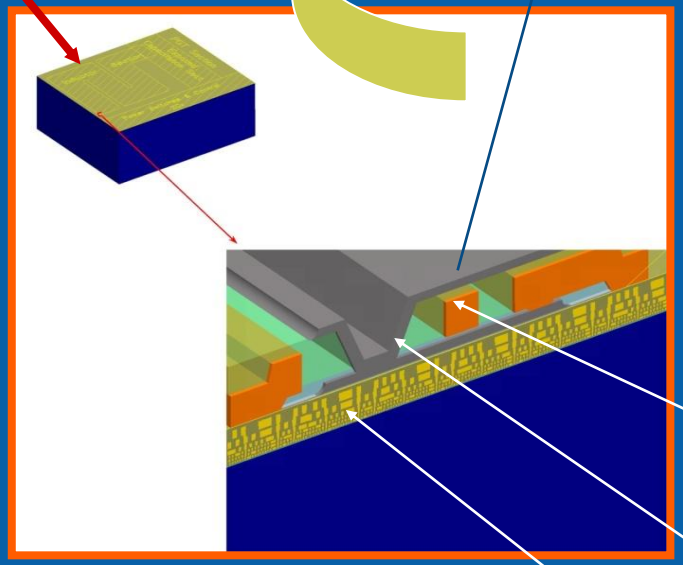
Thin-Film On-die Magnetics



Domain



Magnetic Cross section



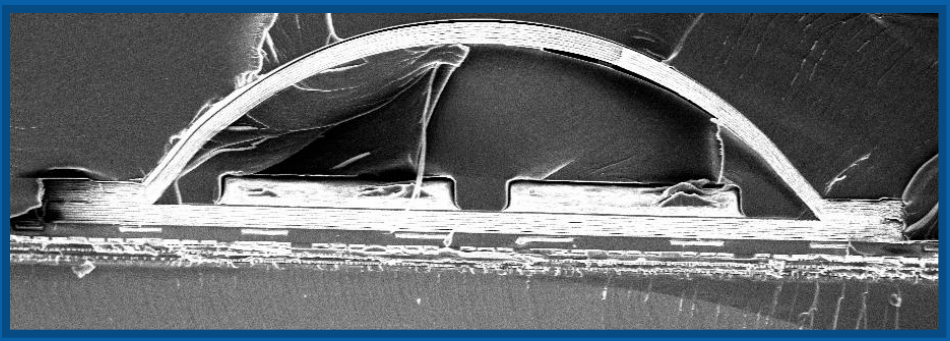
L metal

$Ni_{80}Fe_{20}$

m1-mX

- Technology targets & Stackup
- 90 nm technology for test devices
- 7-8 metal layers + thick metal(C4) + 2 Magnetic layers
- M1-m4/5 routing – bridge connections – decoupling capacitors
- M8 – inductor/transformer interconnect – ~10 um thick metal
- M7,M9 –magnetic material layers– ~4 um thick (laminated) $Ni_{80}Fe_{20}$

Gains from on-die magnetics



Magnetic SEM Cross section

- Energy density increased
- Volume shrinks
- Power Loss decreased

$$W_M = \frac{1}{2}\iiint_{\upsilon} \vec{B}\cdot\vec{H}d\upsilon \cong \frac{B^2\upsilon}{2\mu_r\mu_0}$$

$$\frac{W_M}{W_A} \cong \mu_r$$

$$W_a \cong W_m \Rightarrow \upsilon_m\mu_r \cong \upsilon_a$$

$$\frac{R_a}{R_m} = \frac{P_a}{P_m} \approx \frac{l_m\sqrt{\mu_r}}{l_a}$$

Energy density in thin film magnetics volume compared with air core inductor is proportional to permeability μ_r which is typically > 1000

Thin-Film Magnetics in relation to VR Ckts

- L_{self} ~ 17nH per phase. - K~93%
- 16 phase – 25A/cell Imax
- 2.8 mm² per cell

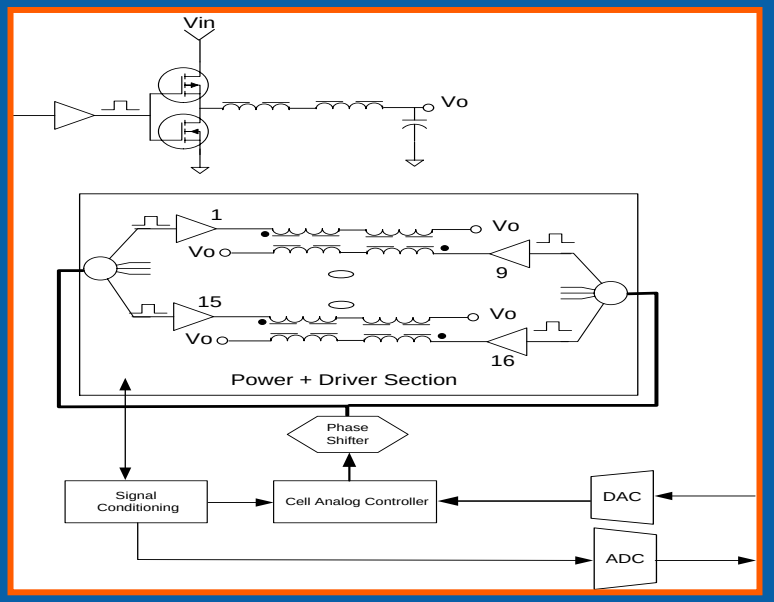
$$P_{L\_c} \cong \Delta I^2 R_c = \frac{\Delta I^2 l_c}{\sigma w_c t_c}$$

$$L \cong \frac{\Delta V \Delta T}{\Delta I} = \frac{\Delta V (1/F) D}{\Delta I}$$

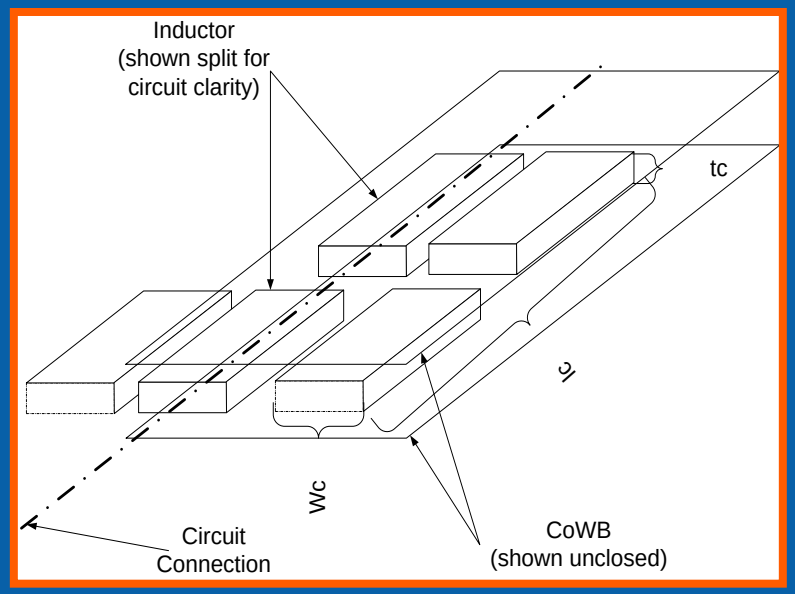
$$* L_{die} \cong \frac{\Delta V (1/F) D}{\Delta I} \cong \frac{B_{Sat} w t_m}{\Delta I}$$

Single Magnetic Top View

Cell Circuit



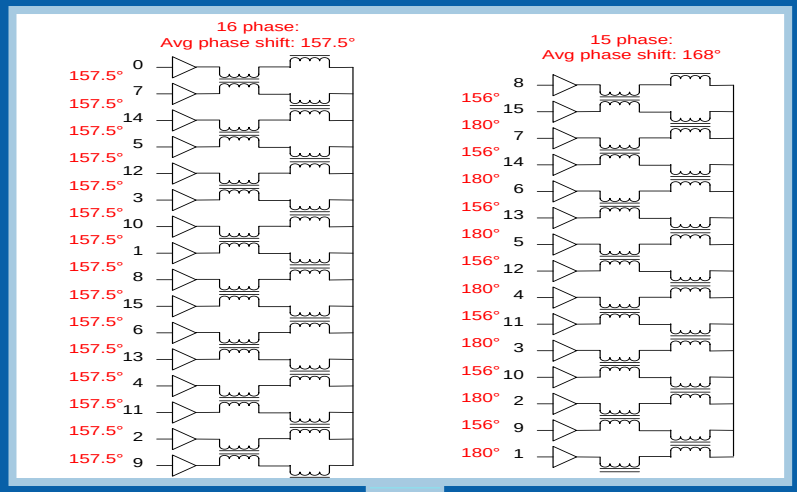
Inductor Physical

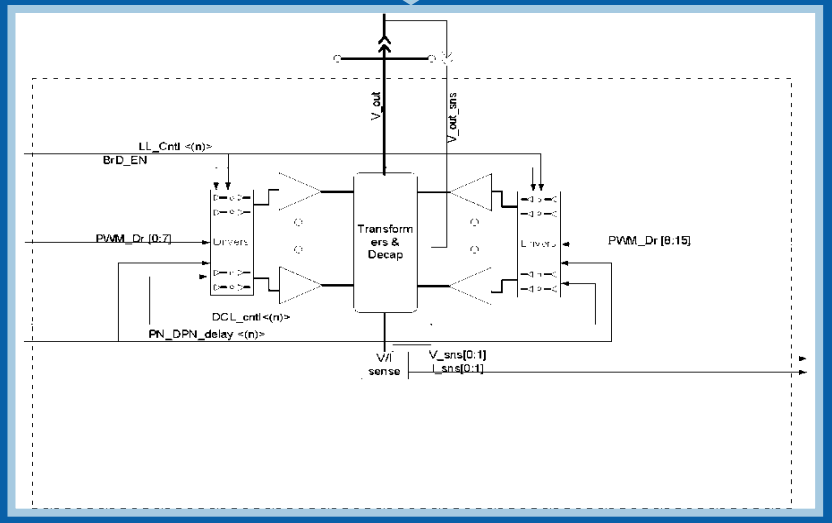


Power Train Architecture

- Cell level power train & Local Controller
- 16 phase 60-140 Mhz (per phase) coupled inductor
- Controller – type I analog
- Current Sense
- Flat efficiency with bridge shedding
- Loop programmable
- Register control between master controller and local cell controller
- Monitor and Observability thru pass-gate port design

16 phase VR



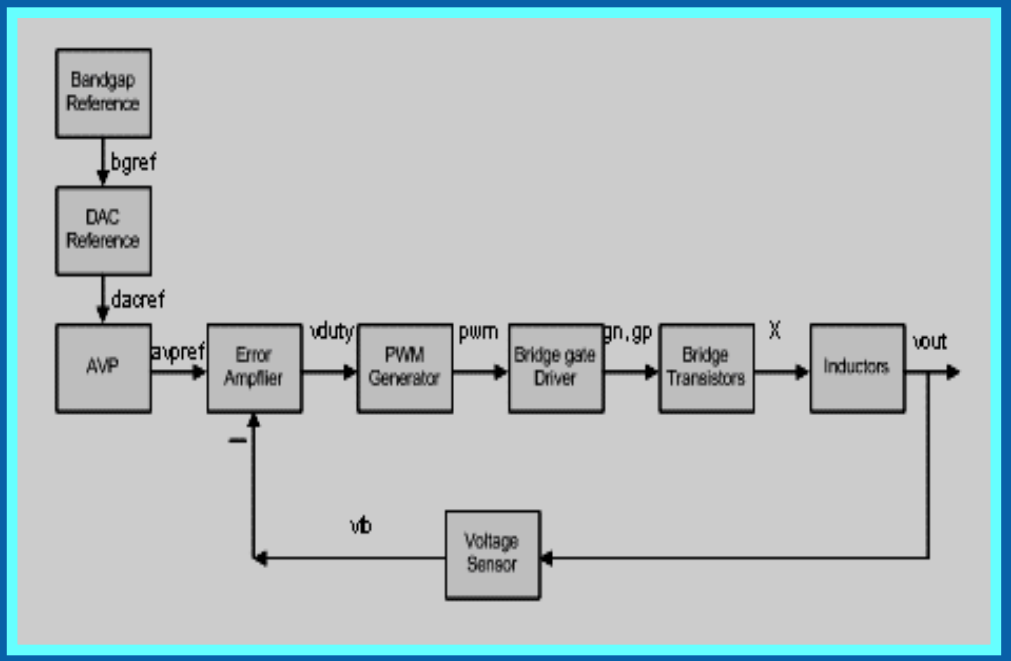


Power Cell Power Train Block

Power Cell Circuits

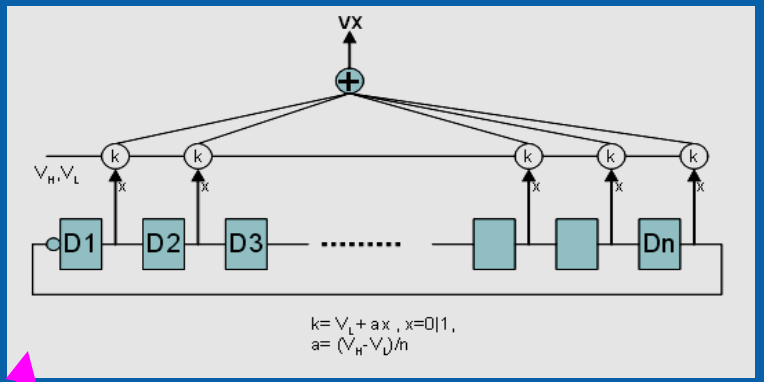
- VR Loop
- Feedback Control
- PWM & Phase generation
- Bridge driver and Transformer
- Reference
- Bandgap with wideband PSR
- VID control D/A converter
- Linear regulators for noise isolation
- Other features
- Synthetic loads – support test activities
- I, V, T sensors

VR Loop circuits



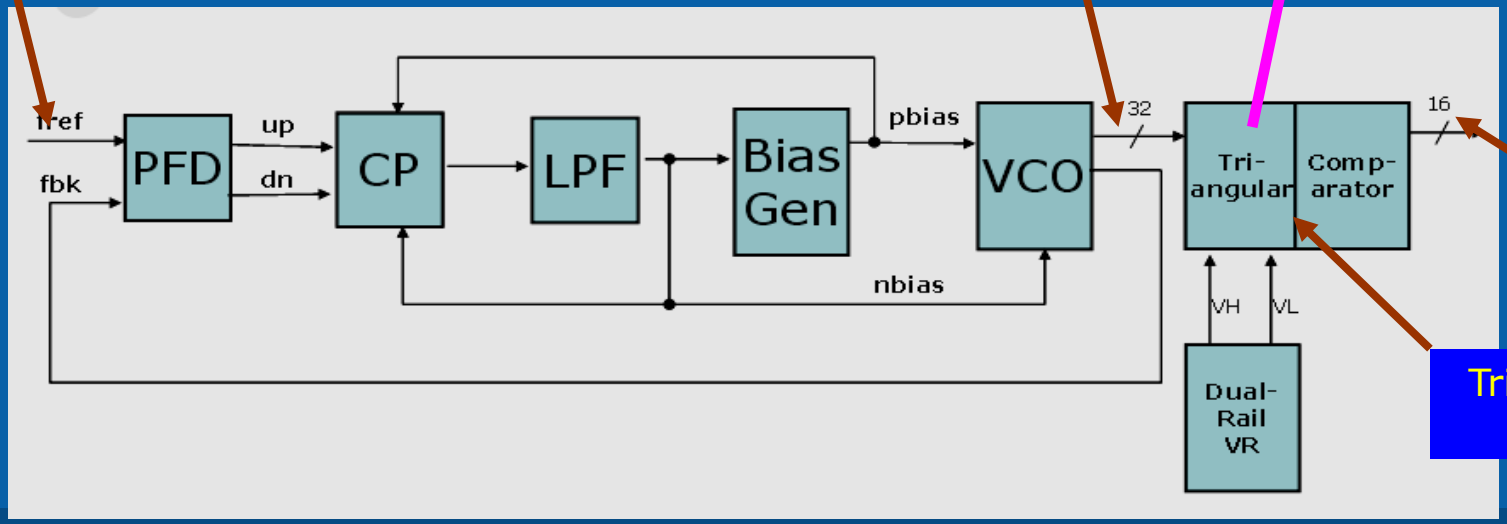
PWM topology

- Differential low power self-biased PLL
- Pulse width control by:
  - Clock => Triangle wave => pulses with variable duty cycle



Ref Clock
1 phase
50% duty

Clock
16 phases
50% duty

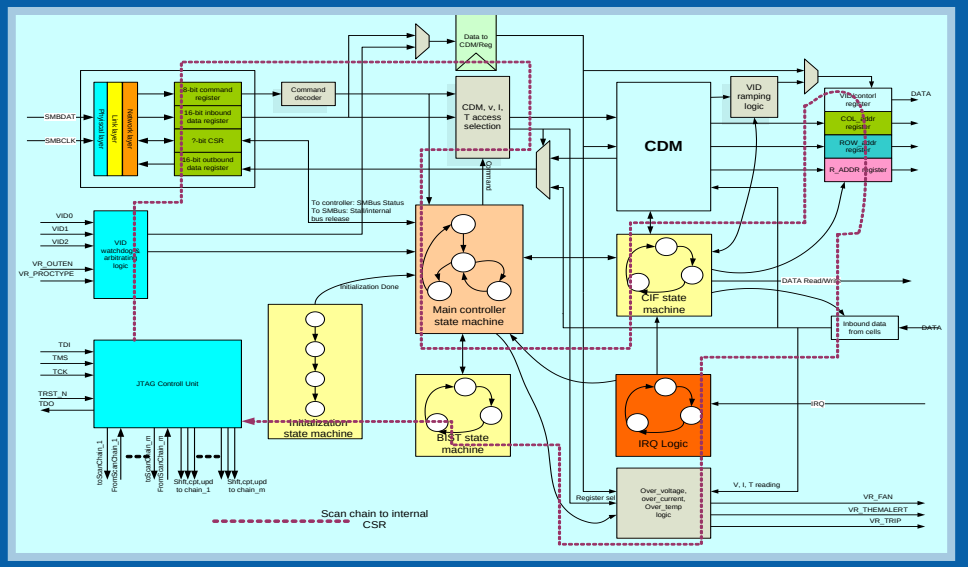


Pulses
16 phases
Variable duty

Triangle Wave
16 phases

Master Control Architecture

- Master Controller Custom RTL
- VID controller
- JTAG 1194 compliant
- Cell Domain Map (V,T,I)
- AVP adjust
- Test & BIST per cell
- Softstart & Warmstart Algorithms
- Internal Buss interface logic
- IRQ buss
- Platform Interface support
  - Parallel buss
- Cell I-balance



Master Controller Block

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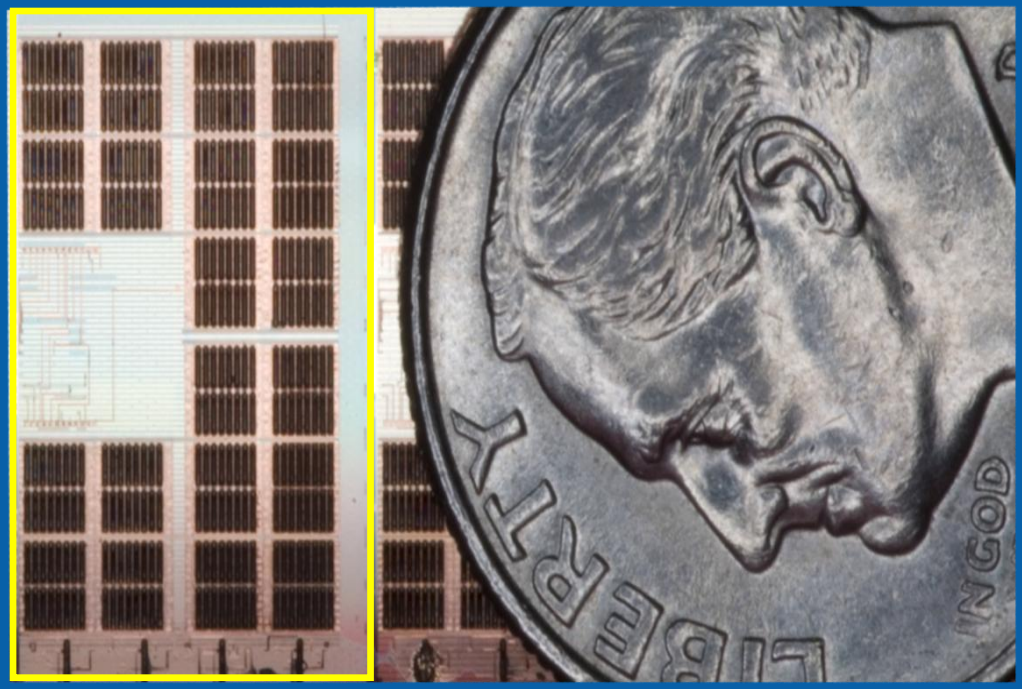
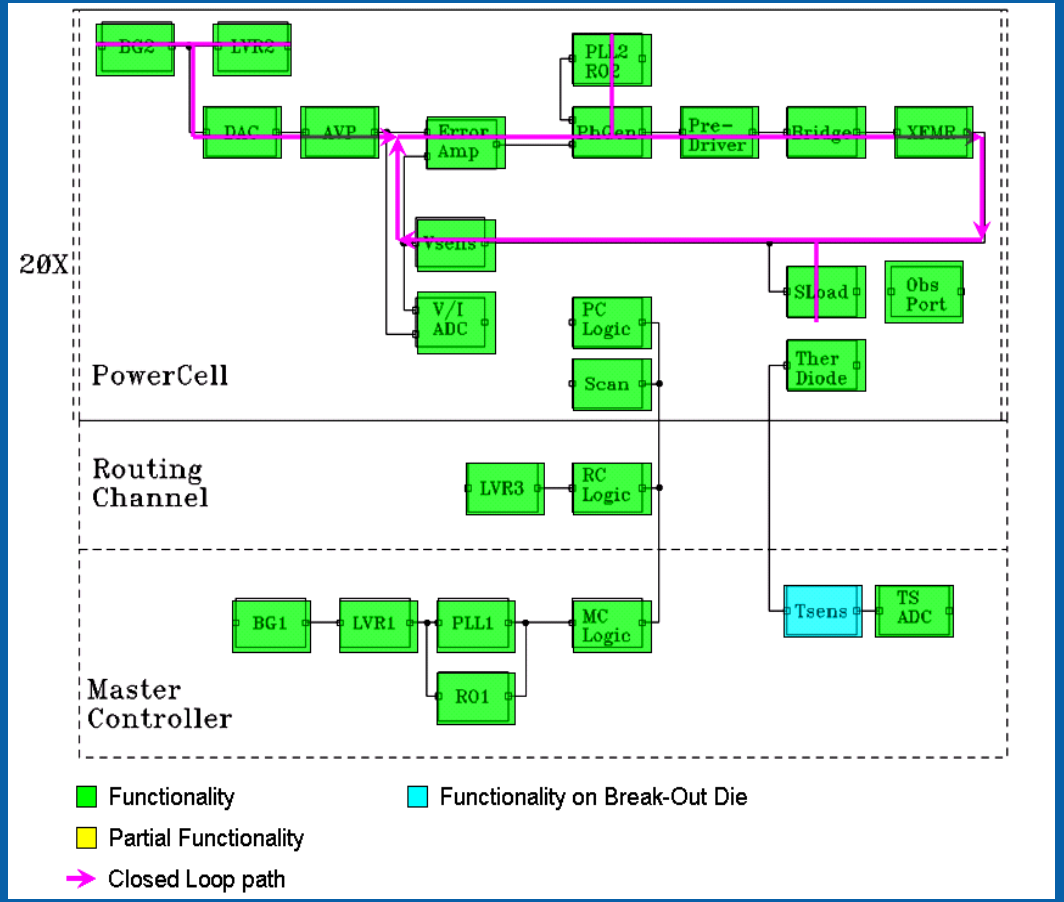


Circuit Testing - Schematically

- Validation
  - Circuits broken down to analog and digital
  - Analog circuits highly observable thru multiple ports
  - ADC and DAC conversions for digital readout
  - Micro-controller testability thru parallel interface and thru TAP interfaces.



Test Results: Snap-shot of circuits – both Wafer Probe & Package

- Bandgap
- All internal linear regulators (LDO's)
- Sensors
  - V/I sensors & ADC used for known-good-die screening –all were functional (not fully debugged though)
  - Temperature sensor and its ADC functional on break-out die
- Interface logic
  - Enabled full programming through either parallel bus or scan
- DFT features
  - such as manual programming of VCO frequency
- Observability ports
  - To look at pre-determined internal nodes

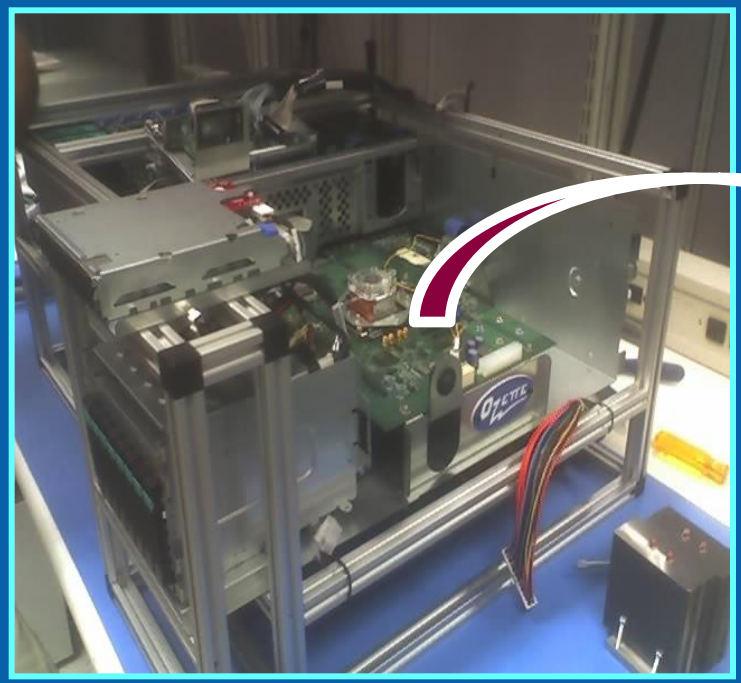
AVP

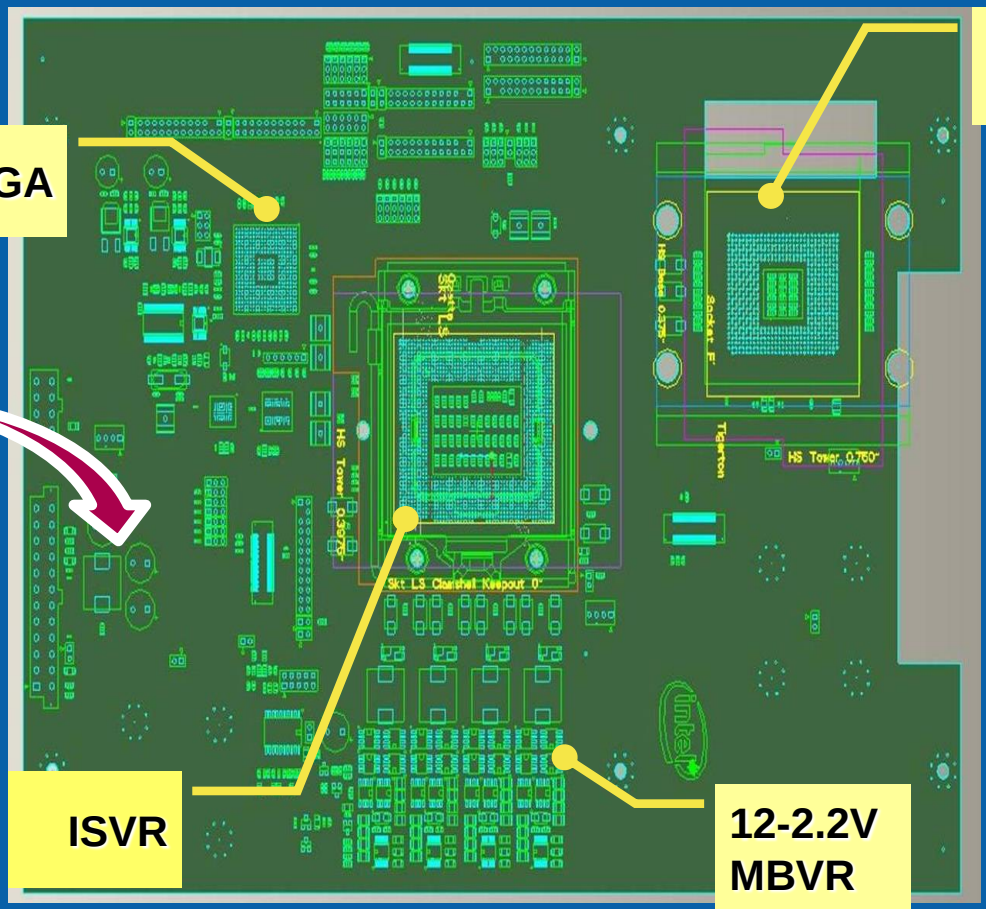
- Shared all 20 Cells

Platform Testing: Interposer & Microprocessor as load

- For testing with CPU and bench testing

Modified Test Platform (Used for booting CPU)

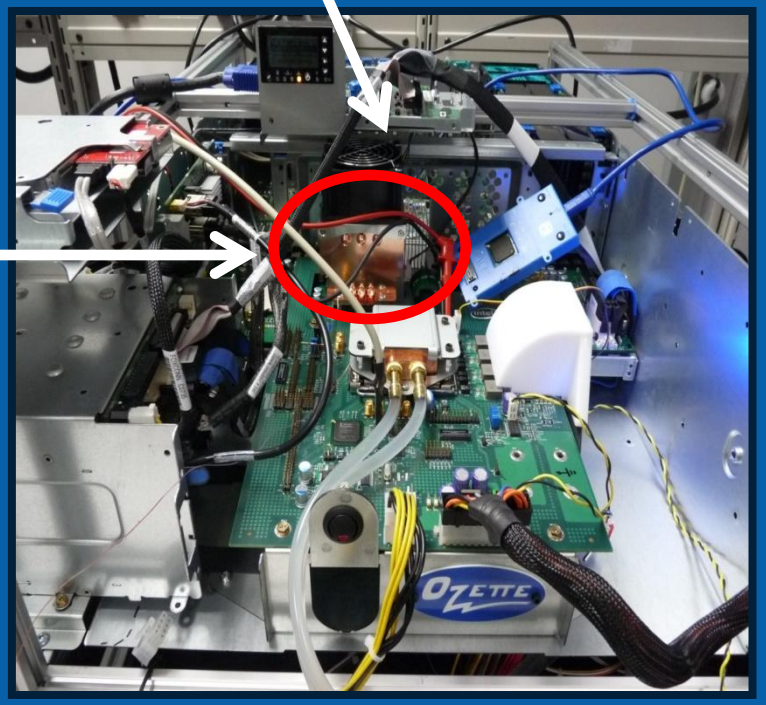




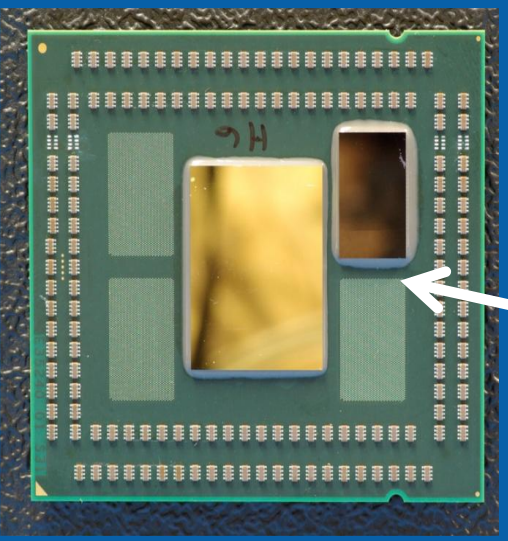
Booted 90W Server CPU – only 3 cells

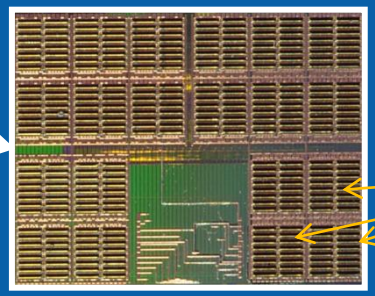
- *Used only 3 Power Cells*
- With 40% of Output Filter Cap*
- Continuous operation with virus for 4+hours
  - No Errors

Intel® Xeon® Processor E7330



Ozette



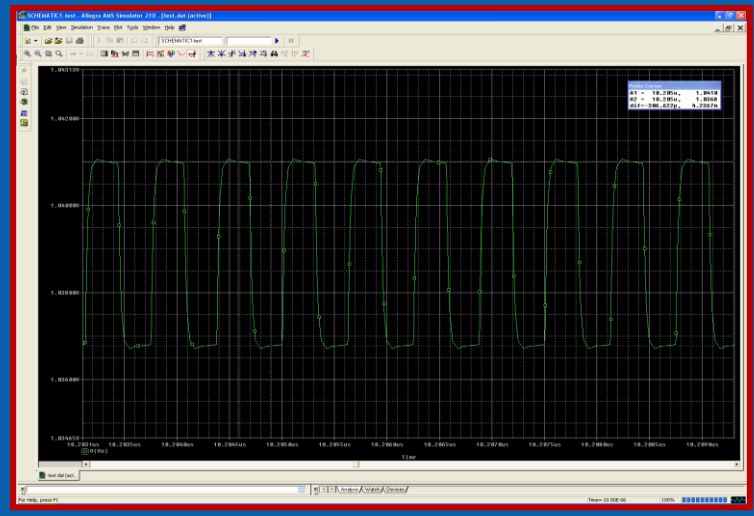


These 3 cells

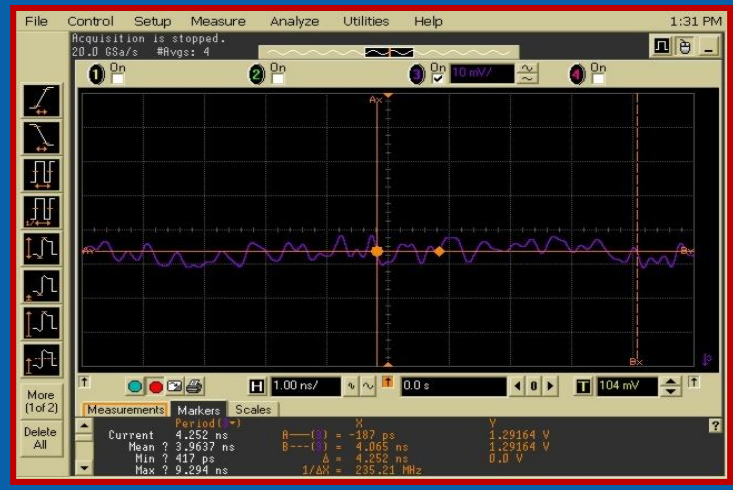
*Compared with MBVR

V_{ripple} & V_{TT}

- Voltage Ripple V_{ripple}
- Measurements in lab on ISVR indicate ripple is almost non-existent
- Simulations yielded worst case *+/-2mv*
- V_{TT} Thermal drift
- Due to thermal time-constant of measurement and error due to linearity circuitry in controller, etc.
- Drift range on package is 60-110C
- Most error is calibrated out and leftover is linearized over temperature range to less than *1mV*



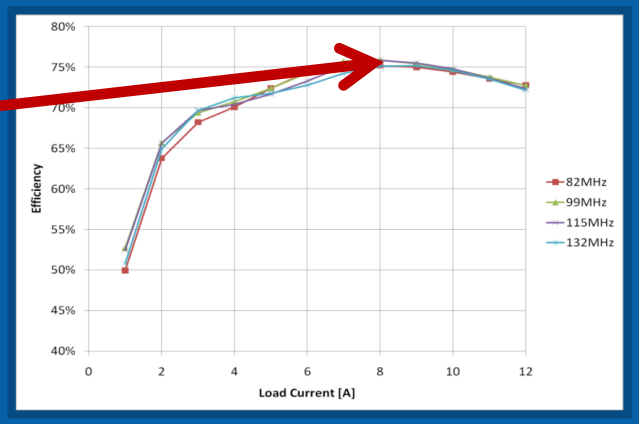
2mV > V_{ripple} sim on Cell



V_{ripple} measurement – Only noise pickup

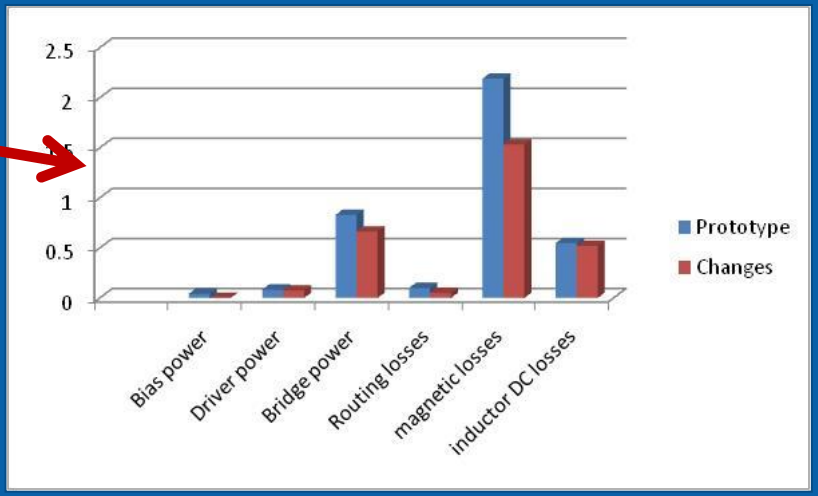
Efficiency – one cell - WIP

- Basic Test (no changes) ~76% peak
  - No bridge shed enable (flat efficiency algorithms not enabled)
  - Bias circuits all on.



'Raw' Efficiency Measurements

- Efficiency* ~**82%** *speculated* with basic changes for 'product' level intro
  - Inductor topology coupling change
  - Non-lab level magnetics processed
  - Bias pwr re-distributed
  - Driver/Bridge circuits re-biased
  - Non-test bridge/output routing

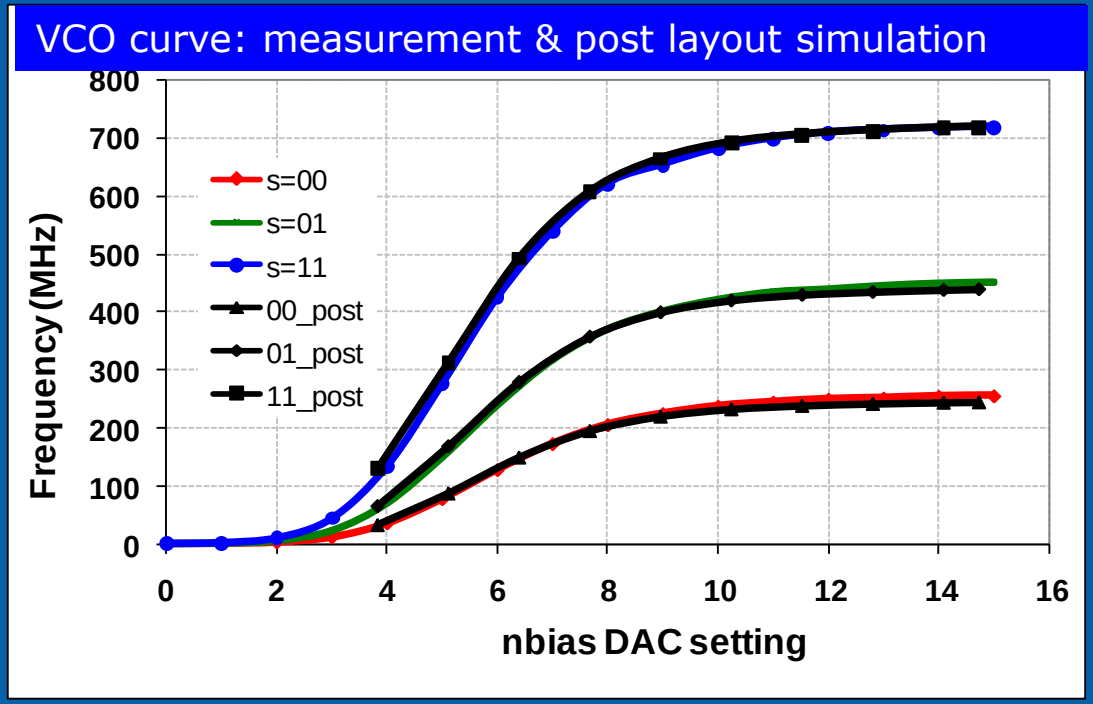


Power Breakdown by element

*Does not include additional advancements that Cannot be reported at this time.

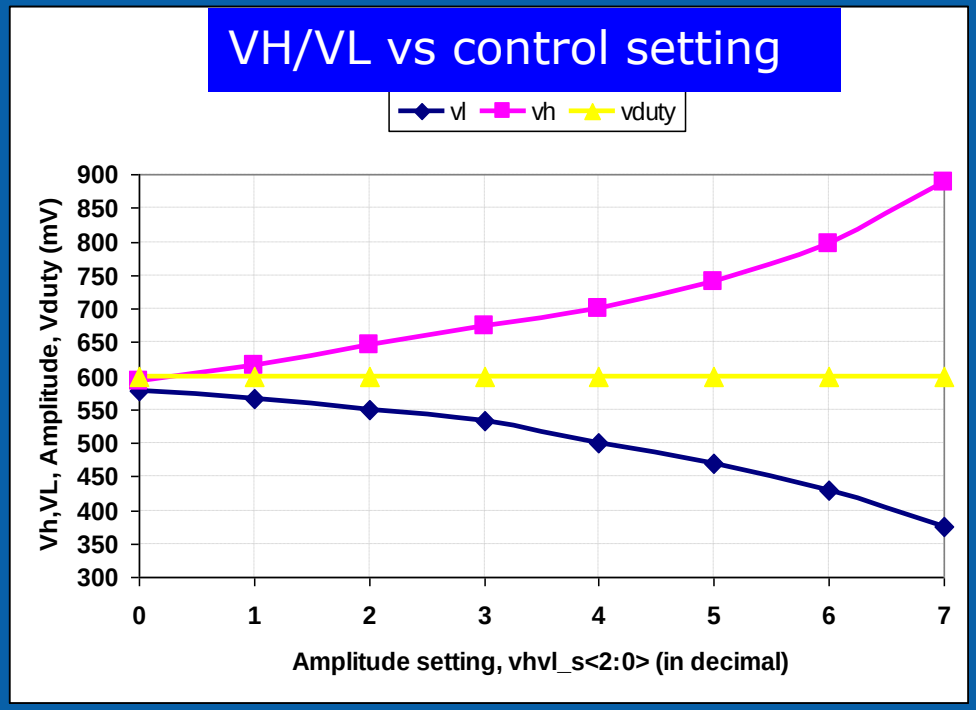
Test Result:
Powercell PLL/VCO

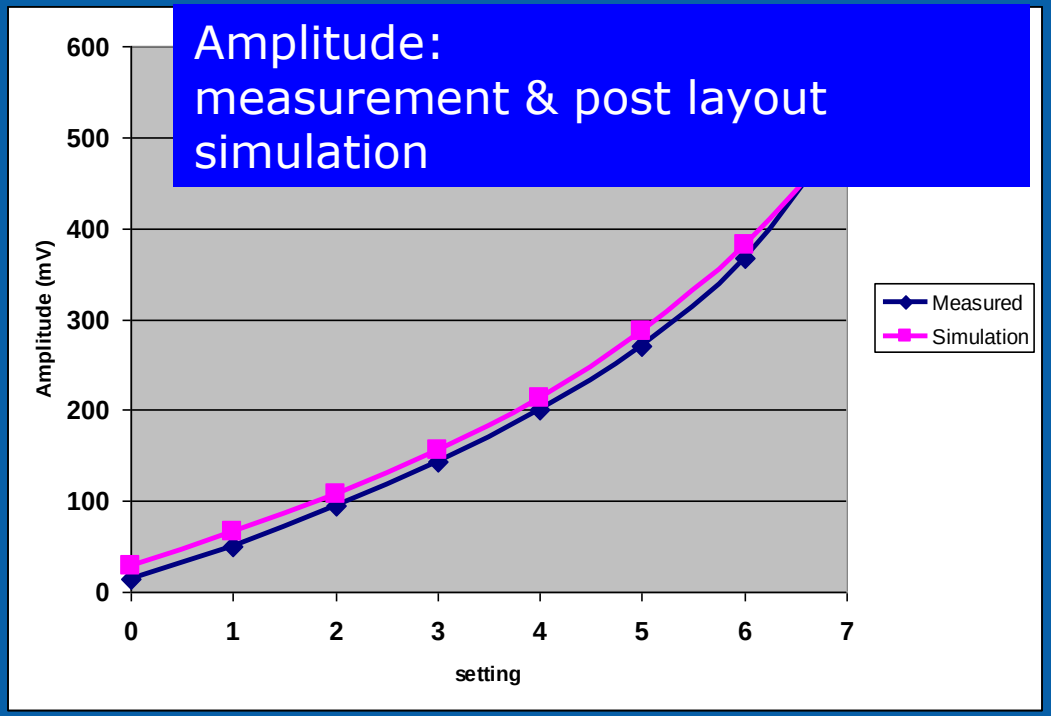
- PLL locking from 20MHz to 200MHz
- Frequencies correlate well with post layout simulation
- Targeted switching frequency, 50-100MHz, is at the linear portion of Kvco curve.



Test Result:
Triangle Wave Amplitude

- Triangle Wave amplitude is set by VH/VL control circuit
- A wide range of triangle wave amplitude can be obtained
- Measurement and simulation matched well





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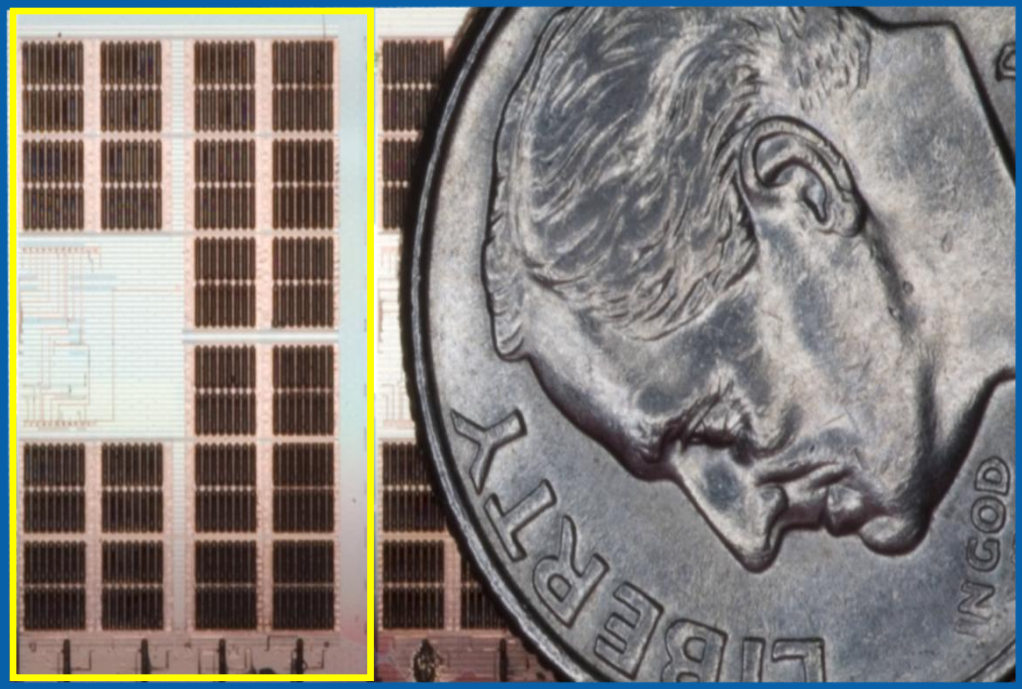


Comparison with other solutions…

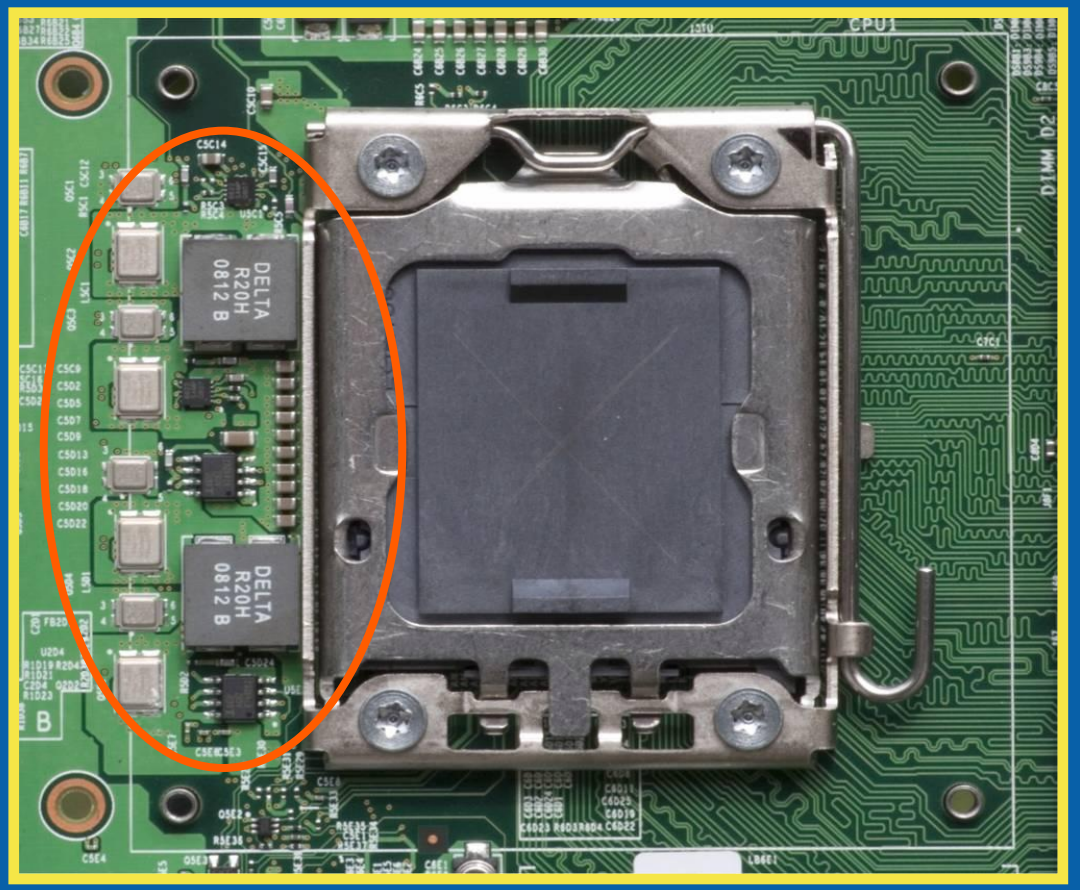
- ISVR vs. Platform VR
  - ISVR is ~400A design; the other is ~120A – input voltages different…but you get the idea.
  - ~110 mm^2 vs. 2700 mm^2
- ISVR technology is ~*50x* smaller

ISVR

~12x9 mm

~18x50 mm

1 ISVR + small 12-2.4V VR replaces 3.2 of these!



VR for Intel® Xeon® Processor E7330

Conclusions

- 400A capable – tested to 220A for less than ½ of chip
  - Board thermally limited.
- Booted and ran server processor (90W design) with 2 cells – ran with 3 cells under Linpack™ for 4+ hours.
- Ripple below noise threshold
- Efficiency in low 80's with minor changes
  - Additional changes possible will boost up.
- Density is ~8A/mm^2 thermally constrained

- Questions?