



Demands for High-efficiency Magnetics in GaN Power Electronics

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 - ii) dc conduction
 - iii) ac loss due to skin effect
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600V GaN Switch Products By Transphorm

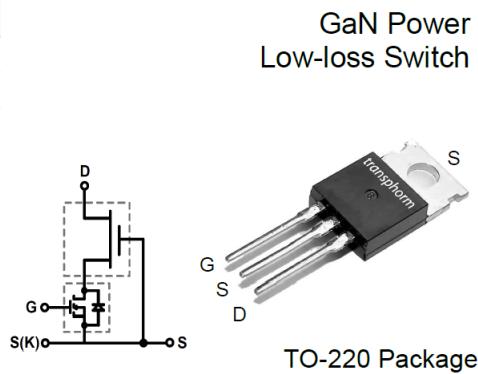
PRODUCT SUMMARY (TYPICAL)	
V _{DS} (V)	600
R _{D(on)} (Ω)	0.15
Q _{rr} (nC)	54

Features

- Low Q_{rr}
- Free-wheeling diode not required
- Quiet Tab™ for reduced EMI at high dv/dt
- GSD pin layout improves high speed design
- RoHS compliant
- High frequency operation

Applications

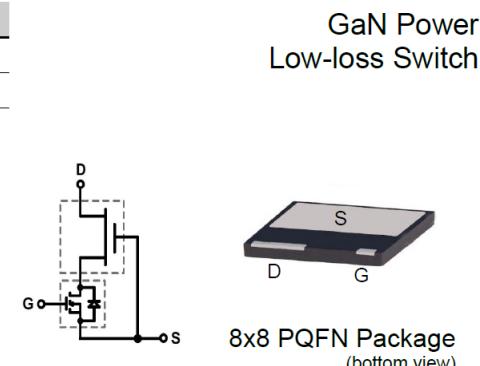
- Compact DC-DC converters
- AC motor drives
- Battery chargers
- Switch mode power supplies



SUMMARY (TYPICAL)	
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- Compact DC-DC converters
- AC motor drives
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Absolute Maximum Ratings ($T_c=25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Limit Value	Unit
I _{D25°C}	Continuous Drain Current @ $T_c=25^\circ\text{C}$	17	A
I _{D100°C}	Continuous Drain Current @ $T_c=100^\circ\text{C}$	12	A
I _{DM}	Pulsed Drain Current (pulse width: 100 μs)	60	A
V _{DSS}	Drain to Source Voltage	600	V
V _{TDS}	Transient Drain to Source Voltage ^a	750	V

First qualified GaN HEMT features very low energy losses

V _{GSS}	Continuous Drain Current @ $T_c=25^\circ\text{C}$	17	A
P _{D25°C}	Continuous Drain Current @ $T_c=100^\circ\text{C}$	12	A
	Pulsed Drain Current (pulse width: 100 μs)	60	A
	Drain to Source Voltage	600	V
	Transient Drain to Source Voltage ^a	750	V
	Gate to Source Voltage	±18	V
	Maximum Power Dissipation	96	W



- 0.15Ω/600V in TO220 & PQFN, S-tab & D-tab
- 0.29Ω/600V in TO220 & PQFN, S-tab & D-tab
- Applications evaluation boards:
 - ✓ All-in-one power supply
 - ✓ Totem Pole PFC
 - ✓ dc-ac inverter
 - ✓ Bridge converter

1st Gen 600V GaN-on-Si HEMT Compared to Si Super Junction MOSFET

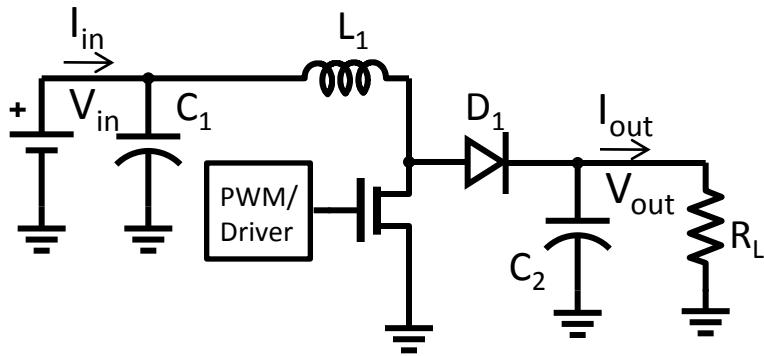
Devices	Parameters	On resistance (Ω)	Gate charge (nC)	Output charge (nC)	Energy related Coss (pF)	Reverse recovery charge (μ C)	FOM1A	FOM1B	FOM2
		Symble	Rds, on	Qg	Qoss	Coer	Qrr	$R_{on} \times Q_g$	$R_{on} \times Q_{oss}$
GaN HEMT TPH3006	GaN Gen1	0.15	6.2	52.8	56	0.054	0.93	7.9	8
Si CoolMOS 60R199CP	SJ Si Gen5	0.18	32	86.4	69	5.5	5.76	15.6	990
Si CoolMOS 60R190C6	SJ Si Gen6	0.17	63	127.68	56	6.9	10.71	21.7	1173
Si CoolMOS 65R2250C7	SJ Si Gen7	0.199	20	126.32	29	6	3.98	25.1	1194
Si CoolMOS 20N60CFD	SJ Si for Low Qrr	0.19	95	76.8	83	1	18.05	14.6	190

- 1st generation GaN is already superior to Si
- GaN still has ample potential to improved

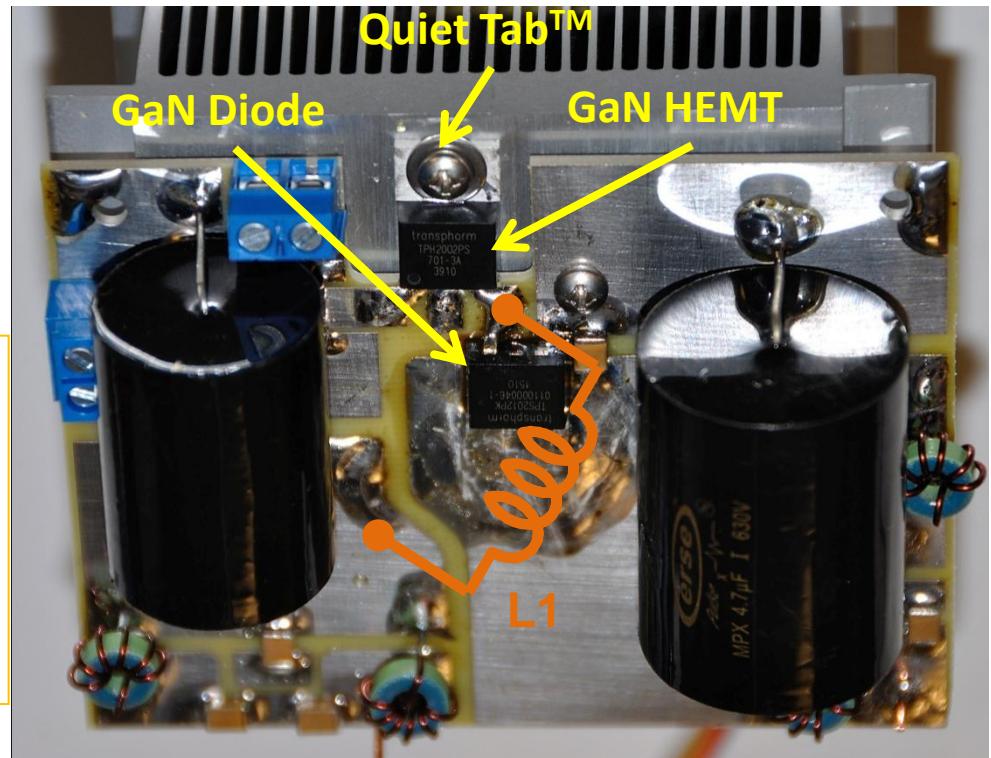
GaN Hard-switched Boost Converter

DC-DC Boost Converter

Converter Schematics



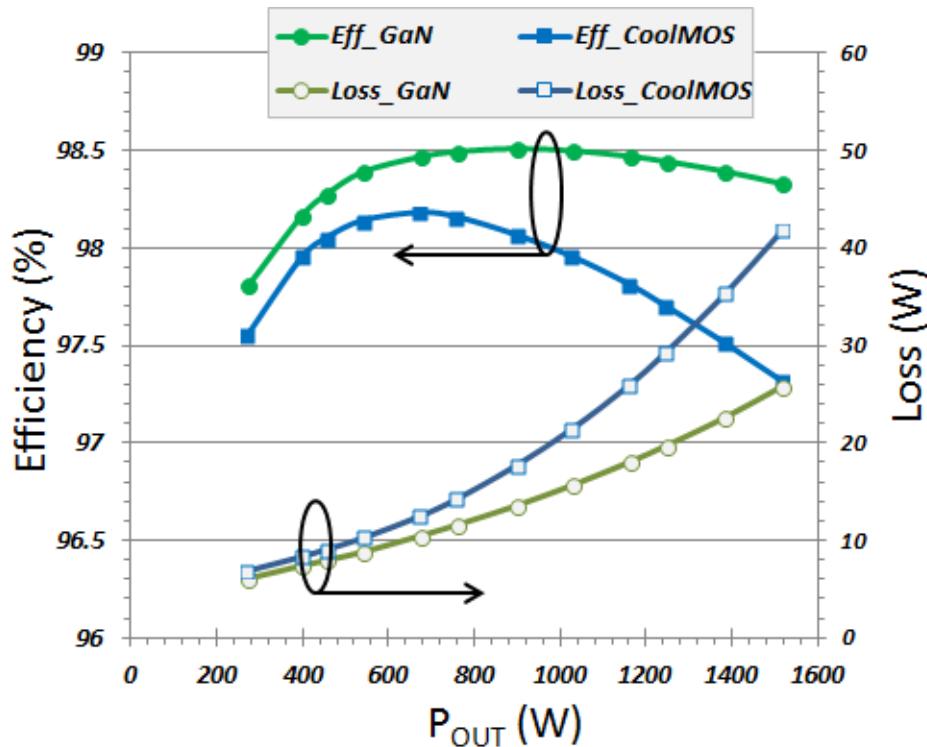
Converter Implementation



- Text-book simple implementation.
- No gate drive compensation network.
- No snubber.
- No insulation shim b/t tab & heat-sink.
- Fast & low ringing waveforms for low switching loss.

Performance of GaN vs. Si Switch in Boost Converter

F=500kHz, 230V:400V



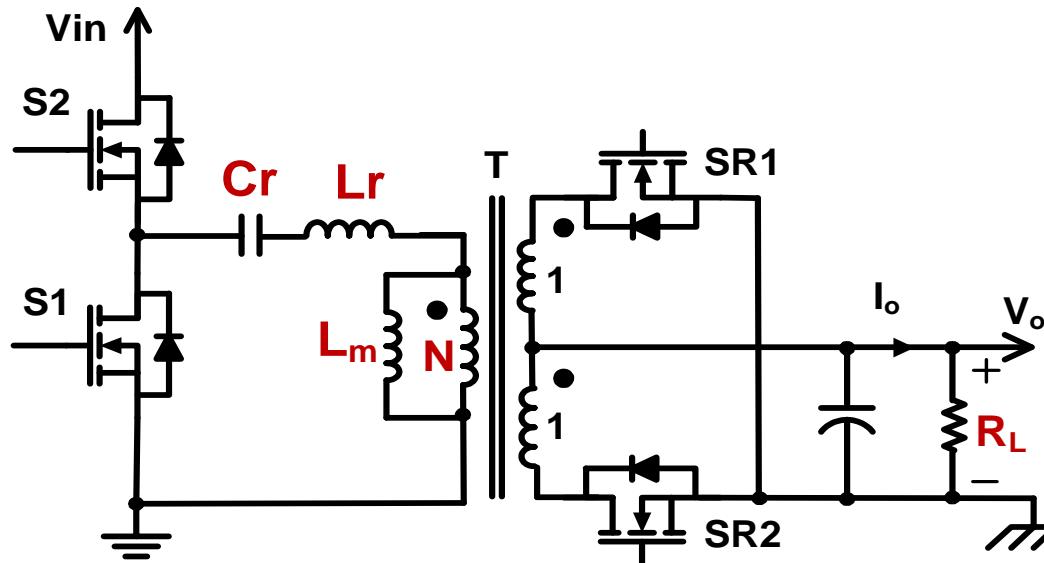
Loss breakdown at 1.5kW

	FET Switch	Diode & Inductor	Total loss
Si (W)	29	9+4	42
GaN (W)	13	9+4	26
Reduction (%)	55.2%	0.0%	38.1%

- Up to 38% overall-loss reduction
- 55% reduction in device loss
- Inductor loss:
 - 9.5% of Si converter loss
 - 15.4% of GaN converter loss

Resonant Circuits Example

LLC DC Converter

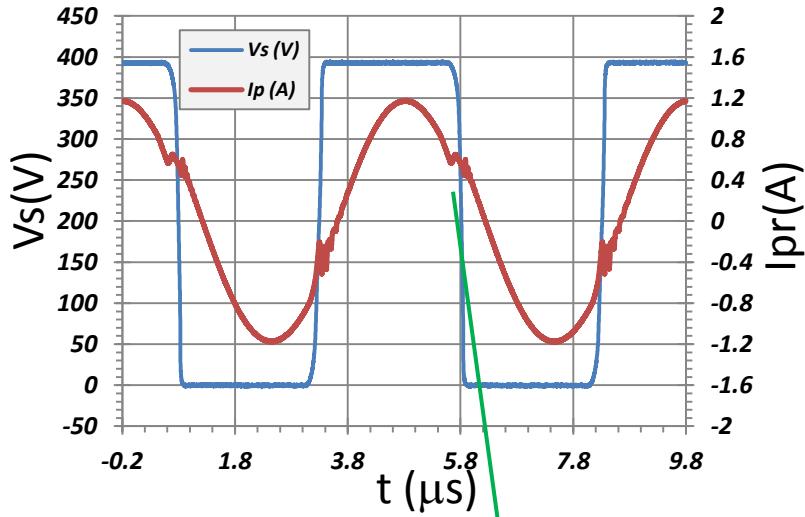


Parameters	Value	Parameter	Value
Vin(V)	400	Vo(V)/Io _{max} (A)	12/25
Lm(uH)	100	Lr(uH)	5.05
Cr(nF)	15	Fr(kHz)	530
Td(ns)	120	Fs(kHz)	470

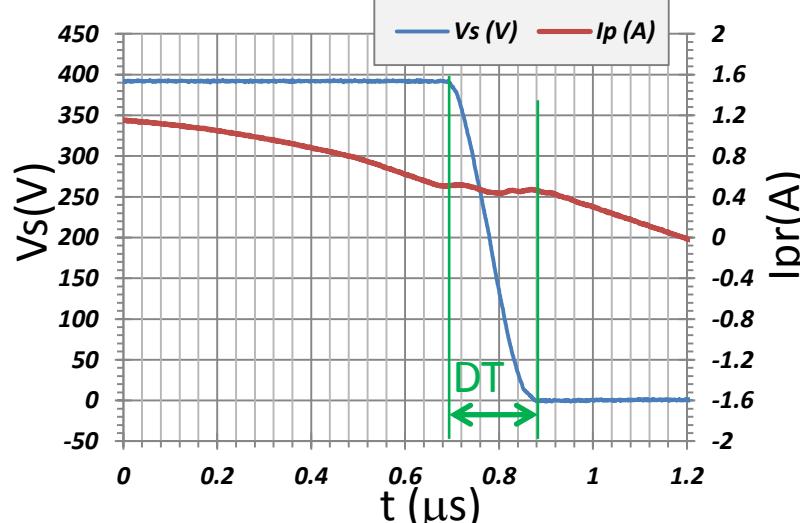
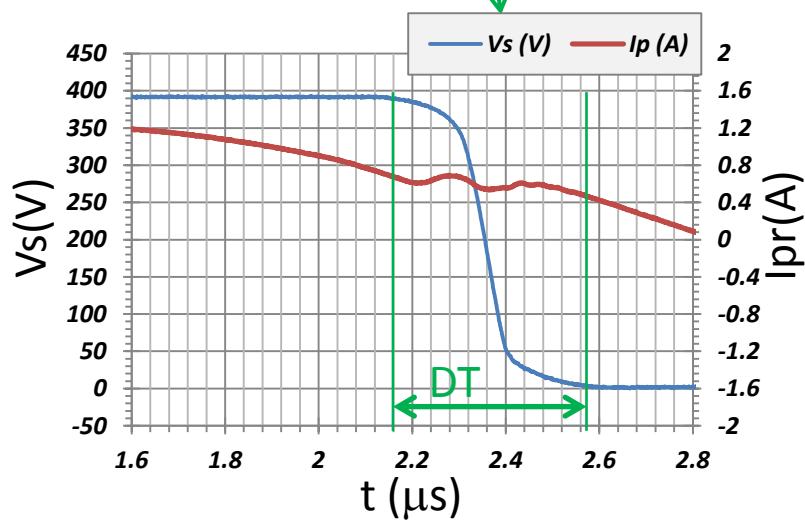
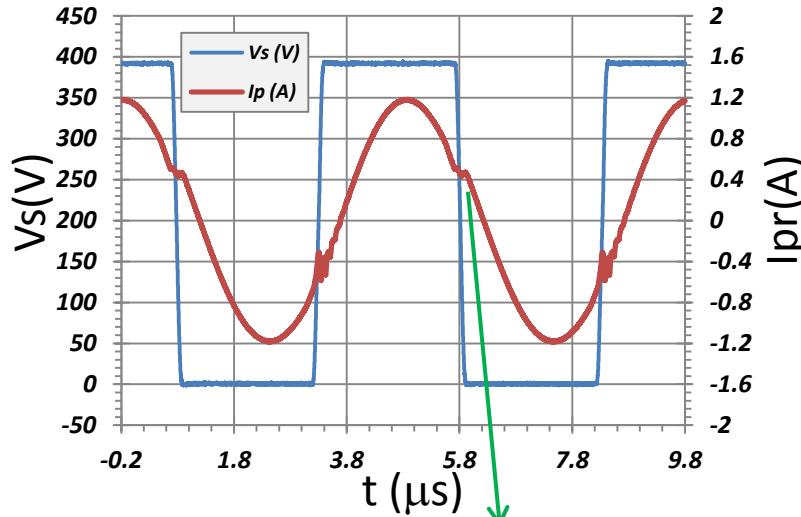
- Low residue charge for GaN allows for a fast reset time & a much reduced recirculation energy

Waveforms of GaN vs. Si in LLC dc-dc Converter

CoolMOS

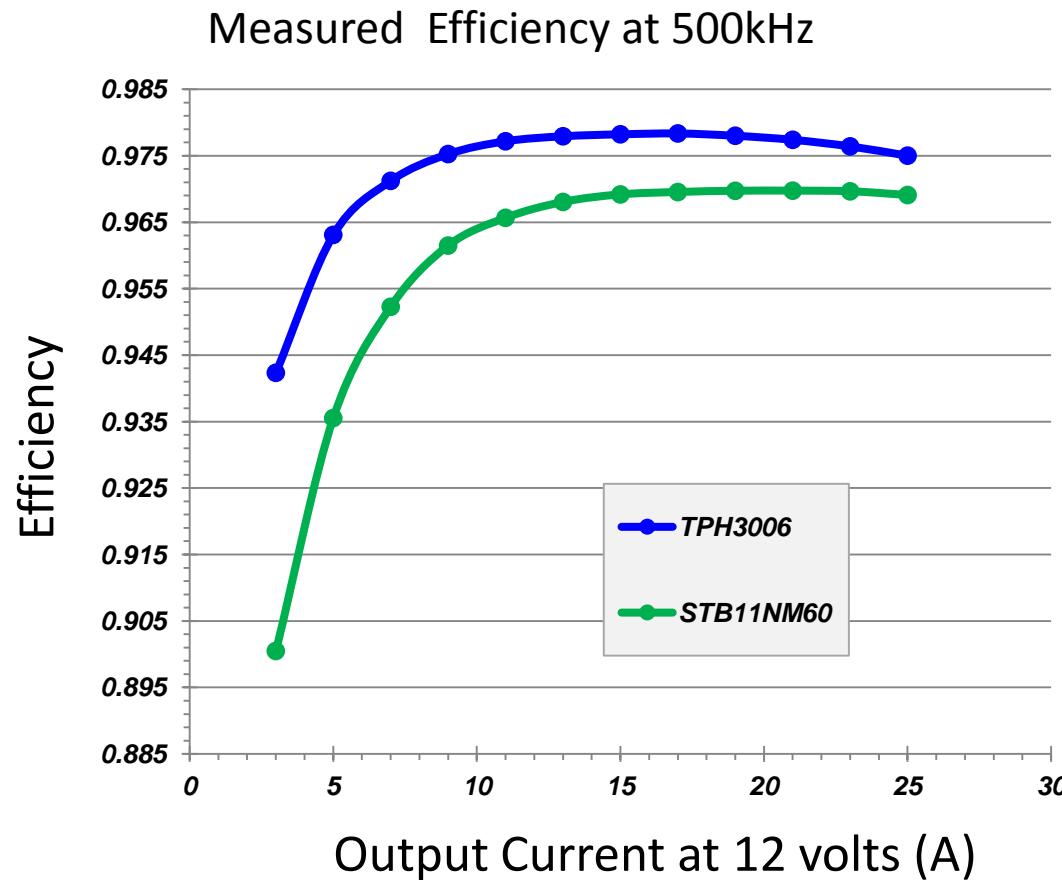


GaN



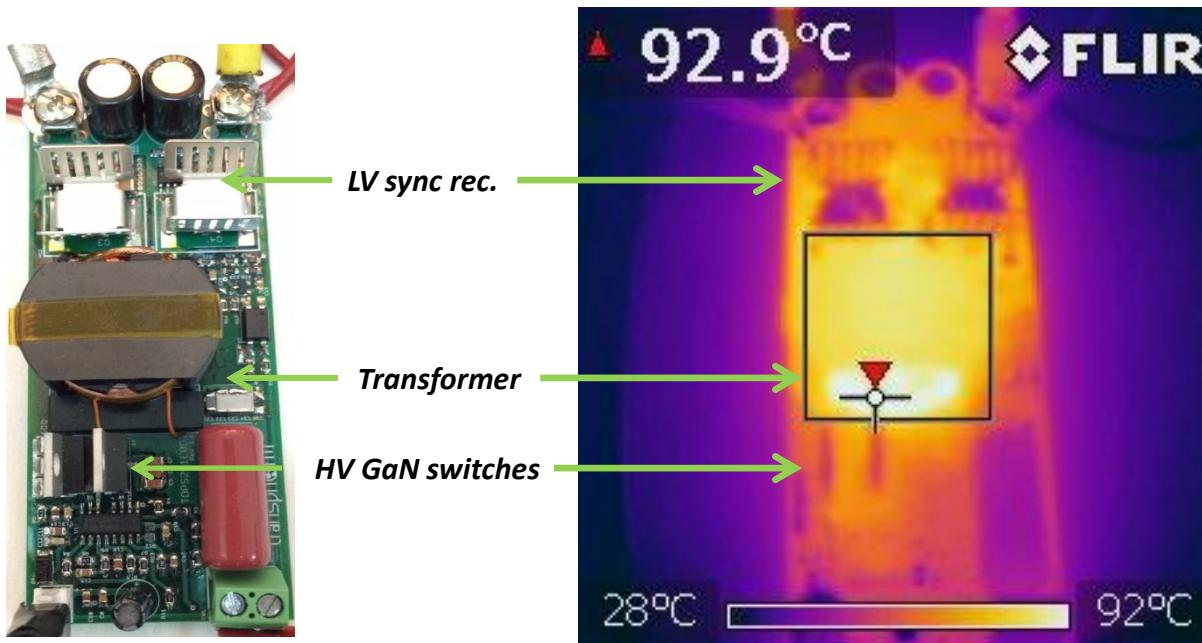
- Si shows large DT: less time for energy transfer: more loss

Performance of High-frequency LLC-DC Converter (open loop)



- 500kHz for compact power supply design.
- Peak efficiency gain by GaN is ~ 0.9% at mid load
- Low-load efficiency advantage is extra high (2-4%)
- Transformer loss becomes very significant at high frequencies

Evidence of Major Power Loss Components (LLC Resonant Converter)



- A compact LLC dc-dc (390V:12V) converter
- $P_{OUT} = 250W$, Eff = 96.5% in open air (peak Eff.=97.7% at 125W)
- Component temperature: transformer=92.9°C, GaN HEMTs=65°C,
Sync rec MOSFETs=75°C,
- Transformer dissipation: >65% of total loss

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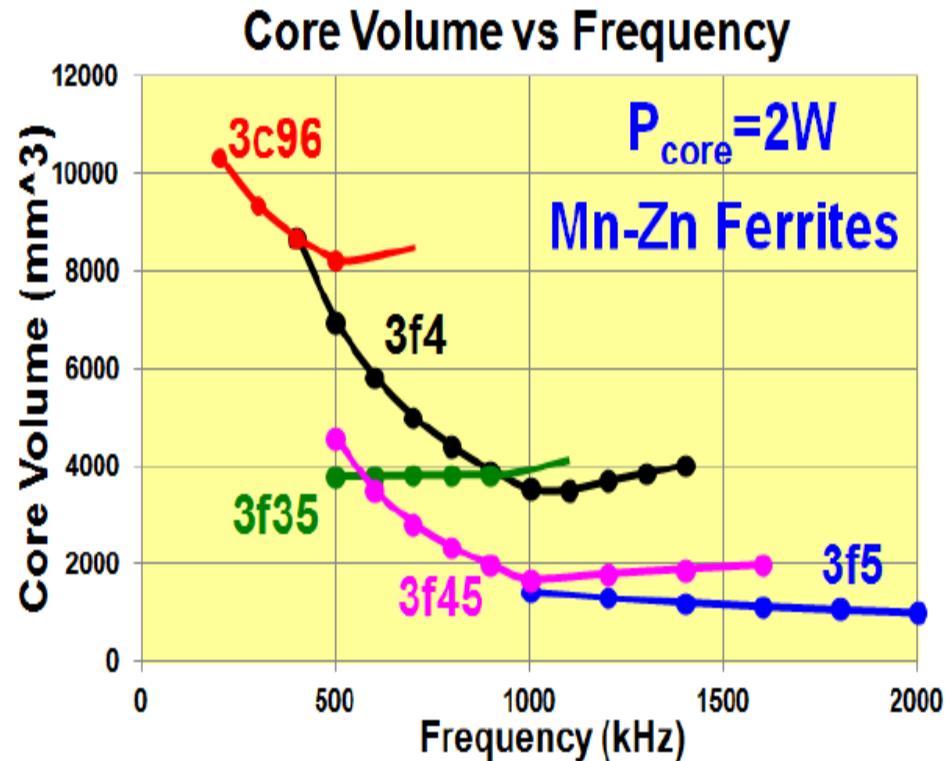
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Generally Accepted Magnetic Core Scaling Rule

$$P_{cv_stein} = k \cdot f_s^\alpha \cdot \hat{B}^\beta$$

$$P_c = V_e \cdot k \cdot f_s^\alpha \cdot \left(\frac{D \cdot V_{in}}{2 \cdot N_p \cdot A_e \cdot f_s} \right)^\beta$$

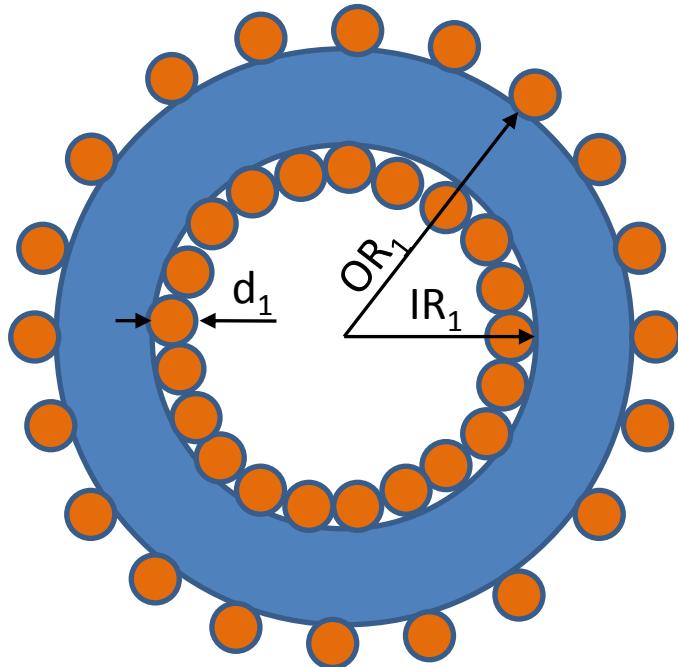
$$V_e = y \cdot \left[\left(\frac{P_{core}}{y \cdot k} \right)^{\frac{1}{C-\beta}} \cdot f_s^{\frac{\beta-\alpha}{C-\beta}} \cdot \left(\frac{D \cdot V_{in}}{2 \cdot N_p} \right)^{\frac{-\beta}{C-\beta}} \right]^C$$



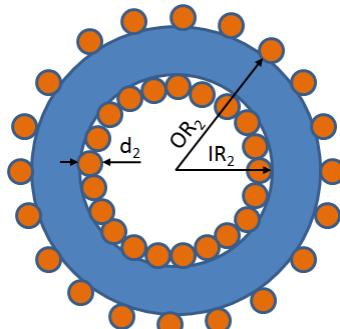
- Assuming constant core loss
- 8x volume reduction from 200kHz to 1.6MHz

Simplified Magnetic Core Scaling: Fixed Core Energy Density

At 100kHz



At 800kHz
1/8 Volume
reduction

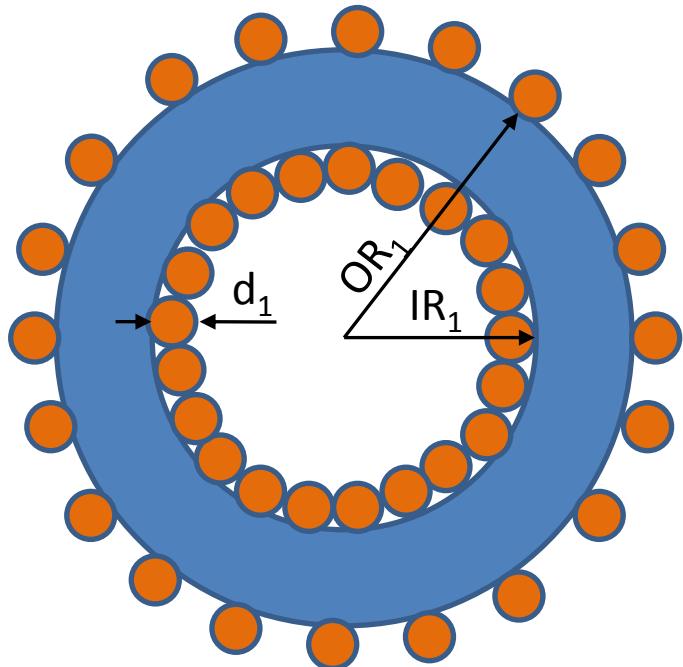


Argument: Constant power storage density per cycle

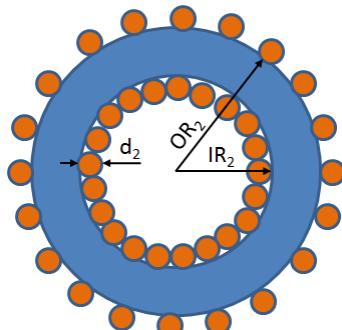
PWM	$f_2/f_1=8$
ac current	$\Delta I_2/\Delta I_1=1$
Inductance	$L_2/L_1=1/8$
Core volume	$V_{m2}/V_{m1}=1/8$
Power loss	$PI_2/PI_1=1$

Magnetic Core Scaling Problem #1: Thermal

At 100kHz



At 800kHz
1/8 Volume
reduction



Argument: Thermal resistance is inversely related to surface area

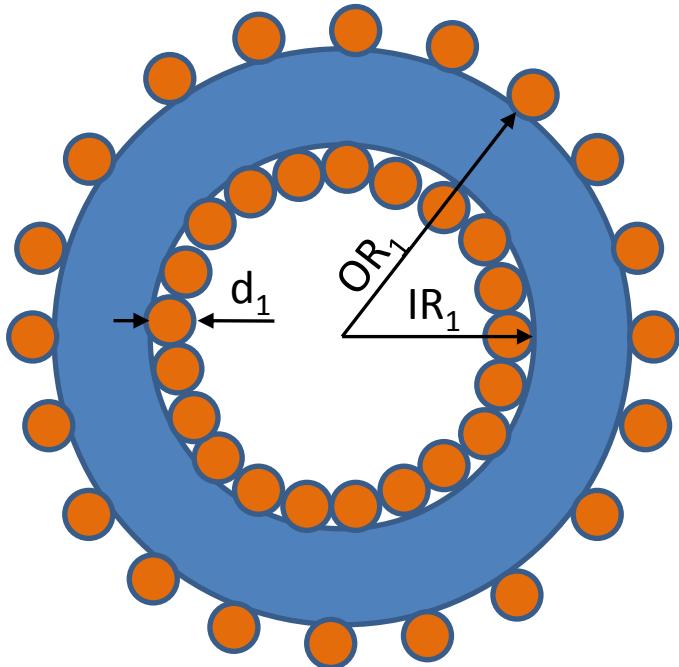
Surface area $A_{s2}/A_{s1}=1/4$

Core temp. $\Delta T_{core2}/\Delta T_{core1}=4$

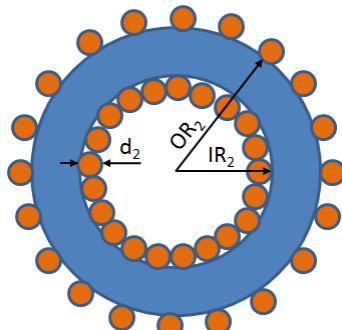
4x high temperature rise!

Magnetic Core Scaling Problem #2: dc Conduction Loss

At 100kHz



At 800kHz
1/8 Volume
reduction



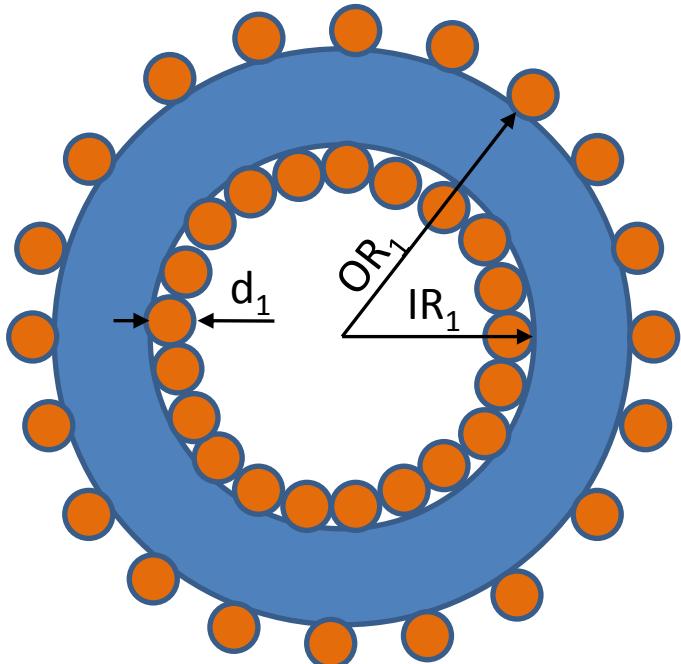
Argument: Ohm's law

Wire length	$l_2/l_1=1/2$
Wire dia.	$d_2/d_1=1/2$
Wire cross section	$a_2/a_1=1/4$
dc resistance	$R_{dc2}/R_{dc1}=2$

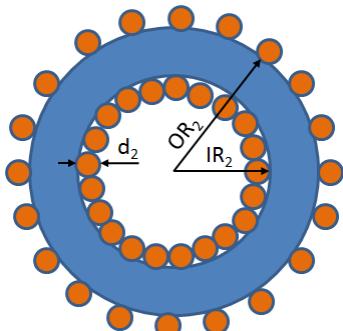
2x dc conduction loss!

Magnetic Core Scaling Problem #2: ac Skin Loss

At 100kHz



At 800kHz
1/8 Volume
reduction



Argument: High-freq. skin effect

Skin depth $\delta_2/\delta_1=1/2.8$

wire periphery $p_2/p_1=1/2$

ac resistance $R_{ac2}/R_{ac1}=2.8$

2.8x ac conduction loss!

Summary

- 1) Better power switches reduce device losses; magnetics become a bottle neck
- 2) 600V GaN-on-Si HEMTs push PWM to higher frequencies allowing much size reduction of power systems
- 2) Although magnetic core scaling expects proportional size reduction with increase in PWM freq., there are multiple hidden issues:
 - i) Core surface temperature is much higher
 - ii) dc conduction loss does not conserve
 - iii) ac skin loss is also increased
- 3) Magnetic material innovation and design optimization are required to minimize above problems
 - i) Magnetic material with low inherent loss at HF
 - ii) Uniform flux winding design
 - iii) Conductor reforming for best spatial utilization
- 4) Material saving by higher PWM is an never-ending push for a sustainable economy